A New Multilevel Inverter Topology with Reduce Switch Count

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Abstract-Multilevel inverters have gained significant attention in recent years due to their ability to generate high-quality output voltage with reduced harmonic distortion compared to conventional inverters. However, existing multilevel inverter topologies often suffer from high switch counts, leading to increased complexity, cost, and power losses. To address this issue, this project proposes a novel multilevel inverter topology designed to significantly reduce the switch count while maintaining performance and efficiency. By reducing the number of switches, the proposed topology offers several advantages, including lower component count, reduced complexity in control algorithms, improved reliability, and lower manufacturing costs. This project proposes a novel multilevel inverter (MLI) topology with 31 levels aimed at reducing the switch count while maintaining high efficiency and improved performance. The proposed MLI utilizes a combination of cascaded H-bridge and flying capacitor cells to achieve the desired output voltage levels. The topology is designed to minimize the number of switches required, leading to reduced complexity, cost, and power losses. A modulation scheme based on pulse width modulation (PWM) techniques is implemented to generate the switching signals for the inverter switches, ensuring accurate output voltage generation and minimal harmonic distortion . The proposed topology is validated through simulation studies using MATLAB/Simulink, demonstrating its effectiveness in generating the desired output voltages with reduced switch count compared to traditional MLI topologies. The results indicate that the proposed MLI offers a promising solution for high-power applications where minimizing switch count is crucial for enhancing system performance and efficiency.

***Key Words*: DC-AC converter, Logical Circuit, Battery ,Cascade H-bridge inverter ,AC Load.**

1. INTRODUCTION

Multilevel inverters (MLIs) are the smart arrangements of dc voltage sources with or without using capacitors and power semiconductor devices to achieve high-quality output voltage. MLIs have been widely studied and are gaining importance in the medium and high voltage power applications. This is due to several important features of MLI such as good output voltage waveforms with a lesser amount of total harmonic distortion (THD), enhanced efficiency, reduced voltage stresses across power devices and better electromagnetic compatibility. Cascaded H-Bridge (CHB), flying capacitor (FC) and neutral point clamped (NPC) are the three basic structures of MLIs. NPC and FC require a higher number of components and issues of capacitor voltage balancing as the number of levels increases. Therefore, many researchers are focusing on the reduction of component count while maintaining a higher number of levels.

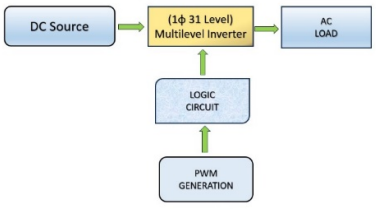

Fig1 Block diagram

An inverter is an electronic device that converts direct current (DC) power into alternating current (AC) power. This conversion is essential for various applications where AC power is required but only DC power sources are available, such as in solar power systems, battery-operated devices, and grid-tied inverters for renewable energy systems. Inverters typically consist of semiconductor switches (such as transistors or thyristors) that switch the DC input voltage on and off at a high frequency, creating an AC output voltage. The output voltage waveform can be modified using different modulation techniques, such as pulse width modulation (PWM), to achieve the desired frequency, amplitude, and waveform quality.

A multilevel inverter is a power electronic device used to convert direct current (DC) power into alternating current (AC) power with multiple voltage levels at its output. Multilevel inverters are used in

applications where high-quality AC voltage waveforms are required, such as renewable energy systems, motor drives, and power grid applications. By producing output voltages with more levels, multilevel inverters can reduce harmonic distortion, improve power quality, and enhance efficiency compared to conventional inverters.

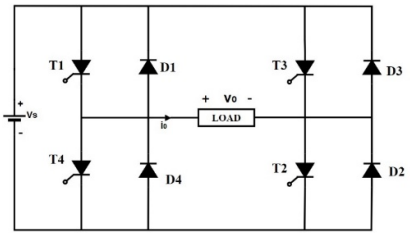

Fig2.Single Phase Full Bridge Inverter

Multilevel inverters have emerged as a key technology in power electronics for high-power applications, offering advantages such as reduced harmonic distortion, improved voltage waveform quality, and increased efficiency compared to traditional two-level inverters. However, one of the main challenges in multilevel inverter design is the complexity and cost associated with a large number of switches required to achieve the desired voltage levels To address this challenge, this project proposes a new multilevel inverter topology with 31 levels that significantly reduces the switch count while maintaining performance and efficiency. The key idea behind this topology is to use a combination of series-connected sub-modules and cascaded H-bridge cells to generate the desired voltage levels with fewer switches.

By reducing the number of switches, the proposed topology offers several advantages, including lower cost, reduced complexity, and improved reliability. These benefits make the proposed inverter topology suitable for a wide range of applications, including renewable energy systems, motor drives, and grid-tied inverters. The primary objective of this project is to develop a multilevel inverter system that offers the benefits of high-voltage conversion and improved waveform quality while simultaneously reducing the complexity and cost associated with switch count. Achieving this goal could significantly enhance the feasibility and scalability of multilevel inverter technology for various applications, ultimately contributing to the advancement of power electronics and renewable energy systems. This introduction sets the stage for the exploration of the proposed multilevel inverter topology, highlighting the motivation behind the project, the challenges it aims to address, and the potential impact of its outcomes on the field of power electronics. Through rigorous analysis and experimentation, this project seeks to demonstrate the viability and effectiveness of the proposed approach in realizing a new generation of multilevel inverters with reduced switch count and improved performance characteristics.

(S. Umashankar, T. S. Sreedevi, V. G. Nithya, and D. Vijayakumar). This paper introduces a novel 7-level symmetric multilevel inverter (MLI) topology that aims to achieve several key advantages over conventional MLI designs. The proposed MLI utilizes only 5 unidirectional switches, which represents a significant reduction compared to conventional 7-level topologies that typically require 9 or more switches. This reduces cost, size, and switching losses. The proposed MLI has a simplified circuit layout, minimizing complexity and making it easier to implement and manufacture. It explains the working principle of the MLI, highlighting how the different switching combinations generate the 7-level output voltage waveform. The paper discusses the use of carrier-based pulse-width modulation (PWM) techniques for controlling the proposed MLI and generating the required switching signals. It also briefly outlines the simulation results using MATLAB/SIMULINK to validate the performance of the MLI

(Maryam Sarebanzadeh, Mohammad Ali Hosseinzadeh, Cristian Garcia). This paper Reduced Switch Multilevel Inverter Topologies for Renewable Energy Sources" published on IEEE Access on Aug 13 2021.Review of conventional multilevel inverter topologies, such as the flying capacitor, cascaded H-bridge, and neutral-point-clamped inverters. They analyze the strengths and limitations of these topologies concerning efficiency, total harmonic distortion (THD), and control complexity. Building upon this analysis, the paper introduces innovative reduced switch multilevel inverter topologies designed to address the identified challenges.

(Thiyagarajan Venkatraman, Somasundaram Periasamy). The paper begins by discussing the significance of multilevel inverters in improving the performance of power conversion systems, such as reducing total harmonic distortion (THD) and improving the quality of the output voltage. The authors introduce a new MLI topology that aims to reduce the number of switches required compared to conventional MLIs. The proposed topology achieves this by using a series connection of a single capacitor and multiple split capacitors to generate the desired voltage levels. The paper concludes that the proposed MLI topology with modified PWM strategy offers a promising solution for reducing switch count in MLIs without compromising performance. The authors suggest that further research and experimentation could lead to practical implementations of the proposed topology in various power conversion applications.

II. PROPOSED INVERTER TOPOLOGY

In this methodology we use battery as the input power supply and the switches are controlled by the help of the gate driven circuit (PWM Pulse) and the gate driver circuit is operated by logical gate circuit. In this circuit we use the 12 switches, inductor and capacitor. These switches are controlled by the logical circuit (AND gate, OR gate). Finally the 31 leveled wave is obtained and by connecting the capacitor in parallel to get pure sinusoidal wave.

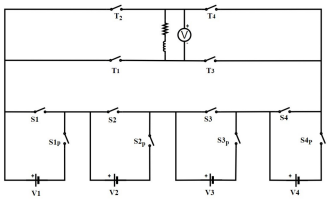

Fig3 Multilevel inverter 31 Level

Conduct a thorough review of existing multilevel inverter topologies, focusing on approaches that aim to reduce switch count while maintaining performance. Based on the literature review, design a novel multilevel inverter topology with 31 levels that significantly reduces the number of switches compared to conventional topologies. Select suitable power semiconductor devices (e.g., IGBTs, MOSFETs) and passive components (e.g., capacitors, inductors) based on the topology and switching requirements. Ensure compatibility with the selected switching strategy and voltage levels. Consider factors such as voltage levels, switch configurations, and component selection to achieve the desired performance. Develop a control strategy tailored to the proposed 31-level inverter topology. This strategy should enable precise voltage control, harmonic mitigation, and efficient operation while minimizing complexity. Use simulation tools such as MATLAB/Simulink to model the designed multilevel inverter topology and control strategy. Simulate various operating conditions and load scenarios to validate the performance and efficiency of the design.

In multilevel inverter the input DC voltage are added in different ways to make the output AC voltage are,

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U1=V1
U2=V1+V2
U3=V1+V2+V3
U4=V1+V2+V3+V4
Un=V1+V2+V3+…. +Vn

The relationship between the number of voltage sources 'n' and the number of levels 'm' during symmetric operation is given by:

$N = M-1/2$ →1

Similarly, the relationship between the number of voltage sources 'n' and the total number of switches 'N_{switch}' during symmetric operation is given by:

$N_{switch} = 2(n+2)$ →2

From (1) and (2), the relation between ' N_{switch}' and 'm' is obtained as:

$N_{switch} = m+3$ →3

III.OPERATION:

The different operating modes of the proposed inverter is shown in Fig. 2. The switches S1, S1p, S2, S2p, S3, S3p, S4 and S4p . T1,T2 and T3, T4 helps to reverse the polarity of the output voltage of the basic unit.. A rectifier unit with an capacitor to filter the DC voltage sources. The proposed inverter can generate 31 level of output voltage during symmetric asymmetric condition.

For the positive half cycle the switch operation are ,During the positive half cycle H-bridge switch T2 and T3 are turn on.

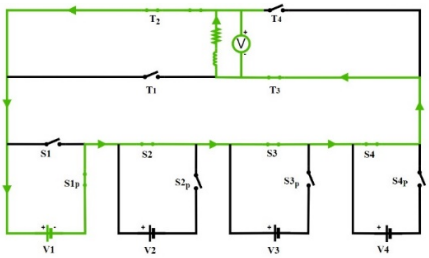

Fig 4. Positive half cycle (V1)

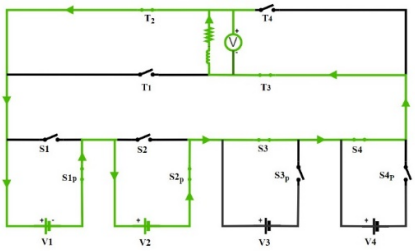

Fig 5. Positive half cycle (V1+V2)

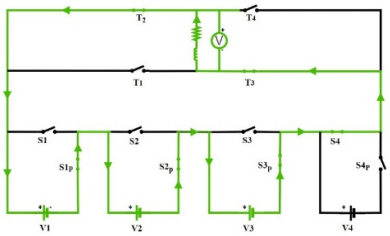

Fig 6. Positive half cycle (V1+V2+V3)

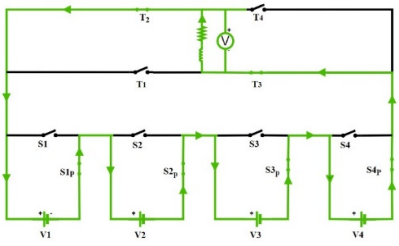

Fig 7. Positive half cycle (V1+V2+V3+V4)

For the negative half cycle the switch operation are , During the positive half cycle H-bridge switch T1 and T4 are turn on.

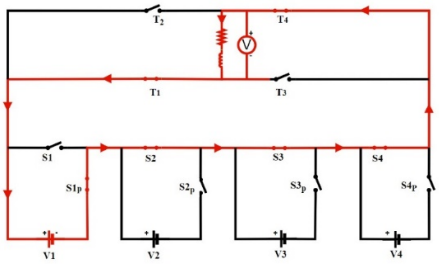

Fig 8. Negative half cycle (-V1)

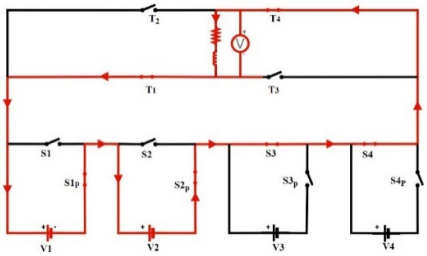

Fig 9. Negative half cycle -(V1+V2)

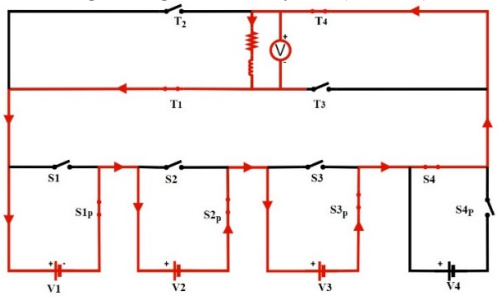

Fig 10. Negative half cycle -(V1+V2+V3)

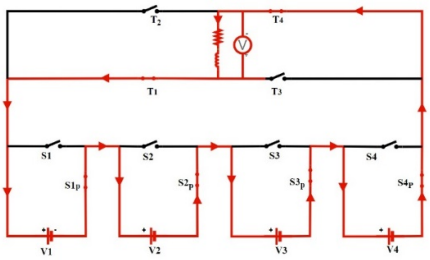

Fig 11. Negative half cycle -(V1+V2+V3+V4)

IV.SIMULATION AND RESULTS:

By using the reference paper and existing model we design the 31 level of multilevel inverter with reduced switch count of 12 switches, inductor and capacitor. Finally, we simulate the circuit of multilevel inverter for AC loads. The logical circuit in the inverter is used to control the inverter switches by using the pulse width modulation (PWM). The logical circuit plays the vital role in the inverter to control the switch operations.

Validate the simulation model by comparing the simulated results with theoretical calculations or existing experimental data. Simulate the performance of the proposed multilevel inverter topology under various operating conditions, such as different output voltages, frequencies, and load levels. Evaluate key performance metrics such as total harmonic distortion (THD), efficiency, and switching losses.To improve the performance of the inverter, such as optimizing the switching strategy or component selection.

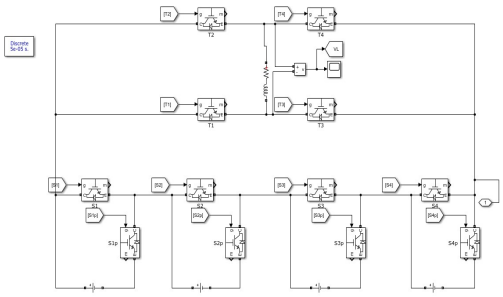

Fig 12. Multilevel Inverter 31 Level

Analyze the simulation results to draw conclusions about the effectiveness of the proposed multilevel inverter topology. Discuss how the reduced switch count affects the performance and efficiency of the inverter compared to conventional topologies.

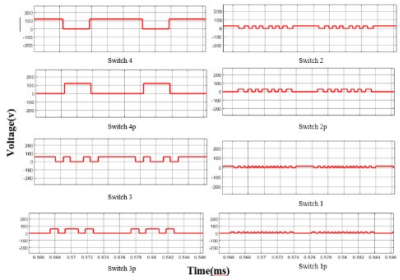

Fig 13 Switch operation

The final output of the inverter

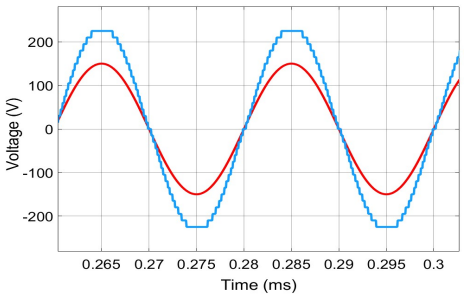

Fig 14. AC Output

V. CONCLUSIONS

In conclusion, the project has successfully designed and evaluated a new multilevel inverter topology with 31 levels aimed at reducing switch count while maintaining performance and efficiency. The proposed topology significantly reduces the number of switches compared to conventional multilevel inverters, leading to lower system complexity, cost, and losses. The simulation results demonstrate that the new multilevel inverter topology achieves high-quality output voltage waveforms with reduced harmonic distortion and improved efficiency. The performance of the new topology has been compared with existing multilevel inverter topologies, highlighting its advantages in terms of reduced switch count and improved performance metrics. The feasibility and effectiveness of the new multilevel inverter topology for renewable energy applications, where high-voltage conversion with reduced switch count is crucial. Finally the proposed multilevel inverter are more efficient for the high precises AC load.

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