CMOS Technology: Conventional Module Design for Faster Data Computations

Charumathi D, Mr.R.Prabhu, M.E.,
PG student, M.E-VLSI DESIGN, Assistant Professor, Dept of ECE,
Gnanamani College of Technology, Namakkal,

ABSTRACT - In this thesis, a family of graph-based algorithms for effectively fast data computation VLSI circuits with basic cells are presented. The first goal of the suggested algorithms is to efficiently reduce the number of logic components needed to implement the synthesized circuit. Next, we devote a great deal of attention on reducing the quantity of inverters needed to connect these logic components. Lastly, this representation of logic is mapped into a circuit that merely consists of the inverters and two-input NANDs and NORS. Optionally, two-input XORs and XNORs may be taken into consideration. Flip-flops are taken into consideration in our work since we also examine sequential circuits. Additionally, the resulting circuits may have some cells with implausible fanout for current technology nodes due to high-effort optimization on the number of logic elements. To ensure that To address these instances, we suggest an area-focused, level-aware fanout limitation mechanism. The suggested methods were used on a collection of reference circuits, and the outcomes demonstrated the method's value. We demonstrate that circuits with fewer simple cells and inverters, when paired with XOR/XNOR-based optimizations, can produce efficient implementations in terms of inverter count, transistor count, area, power, and latency. The suggested methods may be especially useful for these applications since the adoption of a small number of basic standard cells has been demonstrated to be beneficial for a number of contemporary VLSI circuit constraints, including layout regularity, routability, and/or ultra low power limitations. Furthermore, some applications that go beyond Moore, like printed electronics designs, can also profit from the suggested strategy.

Keywords: Graph-based algorithms. logic synthesis. technology fast data computation. standard cell library. simple cells.

1.INTRODUCTION

In today's VLSI industry, design trade-offs include low power consumption, high-speed circuits, and area. The significance of low-power circuit design techniques is highlighted by the development of portable electronics and computer devices. For VLSI designers, low power consumption, minimum latency, and small size are essential design parameters. Reduced power consumption and area are needed in VLSI circuits to improve performance. The fundamental portable device applications for lower power consumption, shorter latency, and increased throughput are the driving drivers behind these designs. Arithmetic operations such as addition are widely employed in low-power VLSI circuits, such as microprocessors and DSP designs for particular applications. These modules are used for a variety of mathematical operations, including subtraction and addition [1]. In light of these facts,Fast data computing circuit designs have low power dissipations, minimal delays, and high speeds [1–15]. A growing number of researchers are focusing on circuit performance with the lowest possible transistor count. The fundamental building component of F-A is the XOR-XNOR circuit. The better performance of the F-A architecture can be considerably increased by improving the performance of an XNOR-XOR circuit.

For search-intensive applications, hardware search engines such as static RAM memory (XNOR-XORs) are significantly faster than algorithmic methods. XNOR-XORs are made up of extra comparison circuitry that allows a search operation to be finished in a single clock cycle, along with traditional semiconductor memory (typically XNOR-XOR). The two search-intensive tasks that Internet routers use XNOR-XORs for the most frequently are packet forwarding and packet classification. I describe the design of XNOR-XOR and circuits by first outlining how lookup is used in Internet routers. Next, we explain how to use XNOR-XOR to create this lookup function.

II.LITERATURE REVIEW

2.1 K. Pagiamtzis and A. Sheikholeslami,-High-capacity XNOR-XOR circuits and topologies are the focus of this system's design. First, we will demonstrate how XNOR-XORs can be used in network routers for packet forwarding in order to spark discussion. Examined the two fundamental CMOS cells—the NOR and NAND cells—at the circuit level. It is also demonstrated how the cells are joined to create an XNOR-XOR word using a match line structure. examined many match line power-saving alternatives to the traditional precharge-high method, such as low-swing sensing, the current-race scheme, selective precharge, pipelining, and current-saving scheme. Additionally, we have examined the traditional method of driving search lines as well as power-saving techniques that use hierarchical search or do away with the search line precharge lines. Three architectural approaches—bank-selection, pre-

computation, and dense encoding—have been examined in order to lower XNOR-XOR power. We have now concluded by outlining our predictions for the future of the XNOR-XOR field.

2.2S. Hanzawa, T. Sakata-The ML sensing circuits must be able to discriminate between MLs with high impedance and MLs with low impedance in order to employ this architecture. Traditionally, this ML sensing has been carried out by first applying the search data on the SLs and then recharging all MLs. Mismatches (MLs with low impedance) discharge to GND, but matches (MLs with high impedance) stay at. Compared to the NAND sensing method, this sensing approach achieves a faster search speed, but at the cost of more power consumption because every cycle, all MLs are charged to and subsequently discharged to GND (excluding given the small number of matching MLs). Furthermore, since one of each pair's two SLs is constantly cycled between GND and, the SL pairs add to the dynamic power usage. Numerous sensing approaches based on the NOR ML architecture have been developed in order to minimize power consumption without sacrificing speed. One method is to lower the ML component of the dynamic power usage by restricting the voltage swing on the MLs to a value smaller than. Reducing the SLs' switching activity is another method for lowering the SL component of the dynamic power usage. We suggested a sensing system that restricts the voltage swing on the MLs in our earlier work. Furthermore, by pre-charging the MLs to GND rather than to, we reduced the requirement for SL reset, which in turn decreased the amount of power used by SL.

2.3.I. Arsovski and A. Sheikholeslami,-An XNOR-XOR architecture with hierarchical search lines and pipelined match lines is proposed. The match-lines are split into two pipeline segments, each of which has a pipeline flip-flop to store the result of the match operation for the segment and an MLSA to determine whether a match exists. Match-line segmentation conserves electricity because it eliminates the need to activate the subsequent segments because the majority of words will miss in the first segment. Low-swing signaling on the SLs is useful for conserving search-line power. For instance, the SL swing might be restricted to output voltage, which is a tiny incremental value over the threshold and corresponds to the NMOS transistor's threshold voltage. This would lessen the When applied to SL, the energy consumption decreases from the original. But the only receivers that are enabled are LSL ones that feed an active ML segment. Disabled are LSLs supplying an idle ML segment. Many match-line segments in a big XNOR-XOR block are inactive, which reduces the amount of search-line power needed.

III.EXISTING SYSTEM

CORE CELLS AND MATCHLINE STRUCTURE

Two primary purposes of an XNOR-XOR cell are bit comparison (specific to XNOR-XOR) and bit storage (similar to RAM). A NOR-type XNOR-XOR cell [Fig. 5(a)] and a NAND-type XNOR-XOR cell [Fig. 5(b)] are depicted in Figure 5. Cross-coupled inverters implement the bit-storage nodes D and in an XNOR-XOR cell, which serves as the bit storage in both scenarios. The bitlines and nMOS access transistors that are used to read and write the XNOR-XOR storage bit are removed from the schematic in order to make it simpler. XNOR-XOR cells usually use XNOR-XOR storage, however other implementations use lower area DRAM cells [27], [30]. In the NOR and NAND cells, the bit comparison—which is conceptually identical to an XOR of the stored bit and the search bit—is implemented in a somewhat different way

MODIFIED XNOR-XOR CELL (4T)

4 nmos transistors make up this modified 4T XNOR-XOR cell design. The cells are organized so that the data is written on two transistors (tw1 and tw0) and stored on two transistors (tc1 and tco)[8]. To store the data, the gates of tc1 („a‟) and tco („b‟) are employed as storage capacitance elements.

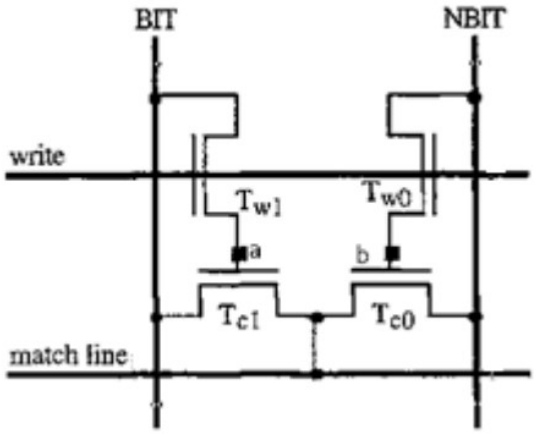


Fig. 7 XOR XNOR-XORcell (4T)

Data can be sent to nodes a and b while transistors tw1 and tw0 are in the ON state. Transistors tc1 and tc0 can then read the data from these nodes.

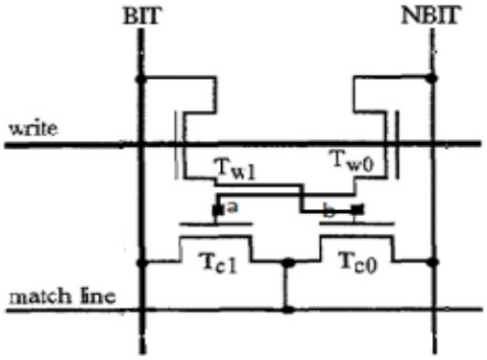


Fig. 8 XNOR XNOR-XORcell (4T)

XOR type transistors, which are arranged using transistors tc1 and tc0, can often be matched using a match line attached to their output. The "data stored" and the "input data" are matched if the match line output is at logic "1." The match line discharges if the output of the match line is at logic "0," which indicates that there is no match. Basically, in order to perform the matching operation, the match line must first be charged to logic "1" using a precharge transistor. The match line must be discharged even in the event of a mismatch, and this can be accomplished by placing a read transistor in between the match line and ground

IV. PROPOSED SYSTEM

Memory-related power dissipation has grown to be a significant issue in contemporary digital design. CMOS technology scaling has resulted in short channel effects. Here, decreased T is used in the design of XNOR-XOR cells to provide greater gate control over drain to source current. XNOR-XOR cells with a 30 nm LG design are employed in hybrid XNOR-XOR architectures with several segments. The original hybrid XNOR-XOR and the results are compared. The suggested architecture's energy measure is found to be 7% lower than that of the hybrid XNOR-XOR.

Static RAM Memory (XNOR-XOR) uses an input that corresponds to the data kept in the memory and an output that points to the content's storage place. XNOR-XOR can be utilized as a search engine to locate content in a database that matches, or A table. A priority encoder is utilized in XNOR-XOR applications where multiple words may match1. Routers and switches work together to create the internet. With the aid of a router, packets are sent from source to destination. A router's job is to link several networks together and verify that packets are sent to the correct location by comparing their destinations. Because lookup operations on routers require quick search times, XNOR-XOR can be used to implement lookup. However, there are trade-offs between power consumption, silicon area, and XNOR-XOR speed. Although the amount of electricity used by ICs is still small, the power per chip is increasing. The future expansion of the industry is at risk if electricity consumption is not decreased. In order to attain performance, reduce power usage, and For years, CMOS devices have been simplifying in terms of portability. Lowering the supply voltage reduces the amount of power consumed, but this causes a number of issues, including punch through, hot electron effect, sub threshold slope deterioration, short channel effects, and drain induced barrier lowering3. In a chip2, memory accounts for 60–70% of overall power usage. One key difficulty with memories is leakage power. Reduced T can ameliorate the very intimidating short channel effect that impacts the device's I-V characteristics as well as the drive current of MOS structures4. This study uses a shorted gate decreased T, where high current drive (ION) is achieved by shorting both gates simultaneously.

Static RAM Memory (XNOR-XOR)

XNOR-XOR is mostly composed of an collection of memory cells. A store unit and a compare unit are present in every cell. The bit is stored in the store unit, which employs Cross-Coupled 6T XNOR-XOR. The search bit and stored bit are compared using the pass transistor logic-based comparison unit. As seen in Figure 1, the XNOR-XOR cell might be of the XOR or XNOR type. The pull-down transistor N5's gate terminal receives the output of the comparison unit. The comparator's output determines whether to switch the transistor ON or OFF. The pull-down transistor is connected to the match line. The match line charges or discharges depending on whether the transistor is ON or OFF. NOR type and NAND type are the two types of XNOR-XOR architectures that are typically used. In every XNOR-XOR Precharge and evaluation are the two stages of the design process. The evaluation phase compares the data in the store unit and compare unit, while the precharge phase charges the match line to a high voltage level.

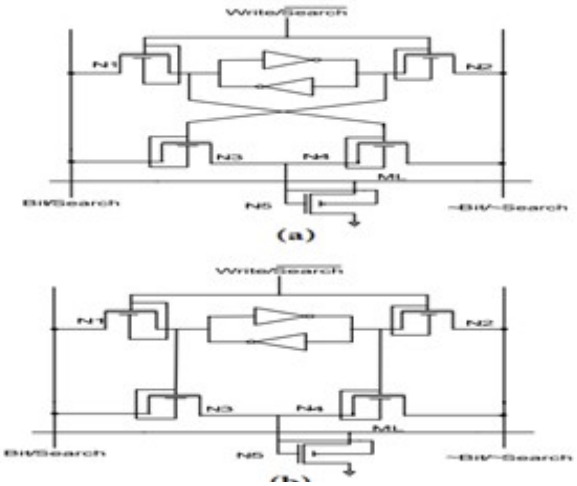


Figure 9.Typical XNOR-XOR Cell. (a) XOR type. (b) XNOR type.

In the era of rapid technological growth, it is essential to develop novel concepts that minimize both the area and power consumption of the cell. Adders are always intended to be the most basic components needed for other multi-core devices and high-performance processes. A quick data processing utilizing a single bit Using a multiplexer and the suggested XNOR cell, eight transistors with a 0.07736W power dissipation have been designed. It is implemented with a custom compiler utilizing 90nm technology and the Synopsys tool (version-L-2016.06-8).

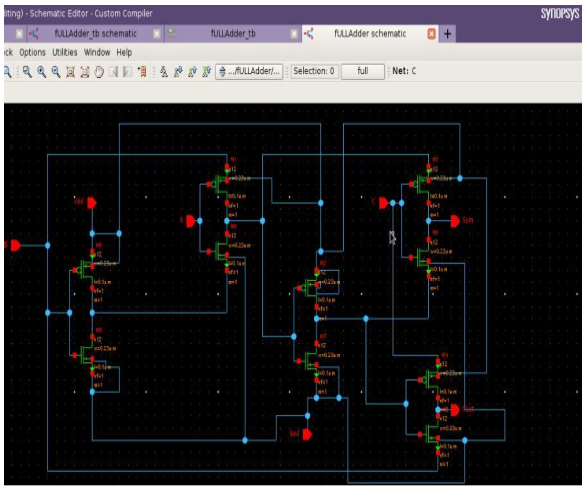
Low power consumption is now a key factor in design. A rapid data computation cell's design criteria are typically multifaceted. Of course, the number of transistors is a major factor that influences the design complexity of several function units, including multipliers and algorithmic logic units (ALUs). Because current battery technology can only deliver so much power, power consumption has become a crucial factor in portable electronics. The size of the transistors, parasitic capacitance, and critical route latency all limit the design's speed. The ability to propel a quick data calculation is crucial since quick data computations are typically employed in cascading configurations, where one's output serves as the input for another. Lack of driving capability in the fast data computations means that more buffer is needed, which raises power dissipation. Fast data computing has significantly improved in the previous ten years in terms of power consumption, speed, and compactness; nevertheless, this development has come at the expense of decreased voltage swing and poor driving capabilities. On the other hand, lower power usage is a benefit of less voltage swing [2].

The development of electronics initially began with the development of vacuum tubes. However, only the mobility of electrons was examined using vacuum tubes. Transistors and diodes were introduced after vacuum tubes. However, for more expansive circuits As they took up more room and power, it was challenging to construct them on a board. The method used to construct the circuit determines how well the quick data computing circuit performs. With the aid of delay time computation, which is directly dependent on the number of transistors, logic depth, and other factors, one can determine an indirect measure of a circuit's operating speed. The quantity, size, and switching activity of the transistors all affect how much power they use. Understanding the area of a die is aided by the transistor size and routing complexity. As integrated circuits increase to very high integration densities and high operating frequencies, low-area circuit realization has become a significant concern. Owing to the significant part that XNOR plays gate in a variety of circuits, particularly arithmetic circuits, when a compact size and delay are required. An optimal design XNOR circuit

V.METHODOLOGY

Conventiona10T Fast data computation:

Fig. 1 displays the schematic of the traditional 10T CMOS fast data calculation.The circuit architecture of the 10T CMOS fast data computation is tailored to use less power and fabrication area while requiring less internal capacitance. Figures 2 and 6 illustrate the respective simulation findings for the output waveform and output power of the 10T fast data computing design using 90nm CMOS technology.



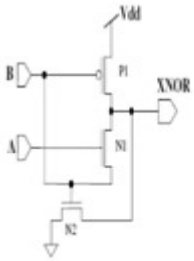
Conventional 10T fast data computation

PROPOSED FAST DATA COMPUTATION:

Basic Building Blocks

1. Three Transistor Xnor Gate:

The logical complement of the exclusive OR (XOR) gate is the XNOR gate (also known as EXNOR, ENOR, and, very infrequently, NXOR, XAND). If the gate receives the same inputs from both sources, a high output (1) is produced. A low output (0) is produced if one or both inputs are high (1) but not both.



INPUTS		OUTPUT
A	B	Y = A⊖B
0	0	1
0	1	0
1	0	0
1	1	1

Fig 2: Existing 3T XNOR GateTable1: Truth table of XNOR logic gate

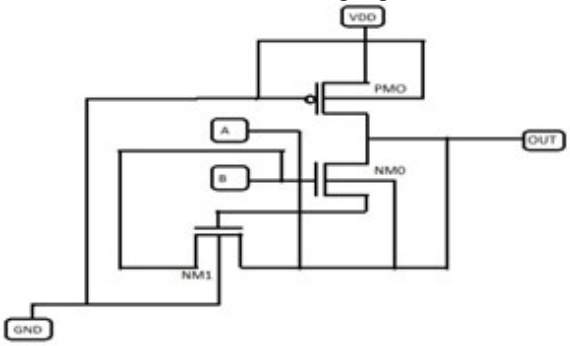


Fig 3: Proposed 3T XNOR Gate

DESIGN & IMPLEMENTATION OF FAST DATA COMPUTATION CIRCUIT

Different combinations of XOR/XNOR modules and two multiplexers can be utilized to create a fast data computing circuit; however, this method has not been applied in current work since XNOR/XOR cells consume more power than a single XNOR gate. As seen in Figure 4, the proposed rapid data computing circuit is constructed using one multiplexer block and two XNOR gates. Two XNOR gates provide the sum, and a two transistor multiplexer block produces the cout. Figure 4 illustrates the implementation of the single bit rapid data computation utilizing the suggested XNOR gates with eight transistors. Typical width (Wn& WP) values of 0.23µm & 0.23µm for NMOS and PMOS transistors with a gate length of 0.9µm have been taken for the multiplexer section With a 1.2V supply

voltage, simulations based on SAE (Simulation and Analysis Environment) 0.9µm CMOS technology have been carried out using SPICE.

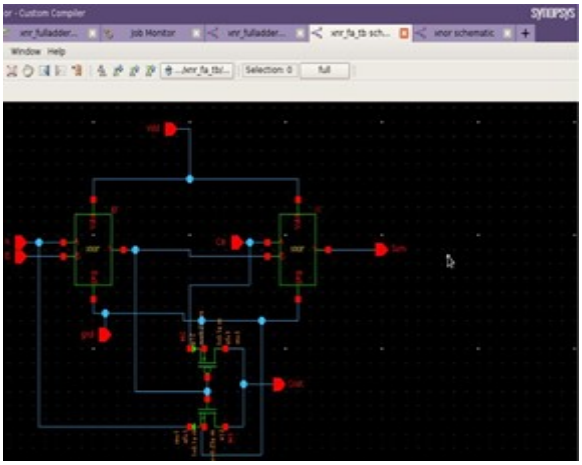


Fig 4: Proposed Fast data computation

VI. EXPERIMENTAL RESULT

Output wave forms of conventional and proposed Fast data computations are shown in Fig 6 and Fig 7.

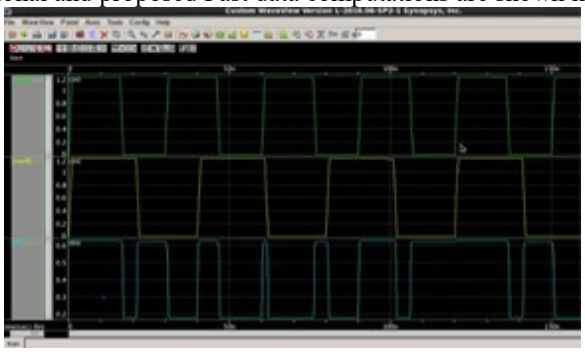


Fig 5: Output Waveform of proposed 3T XNOR Gate

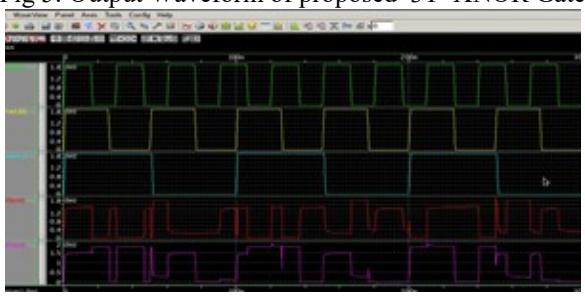
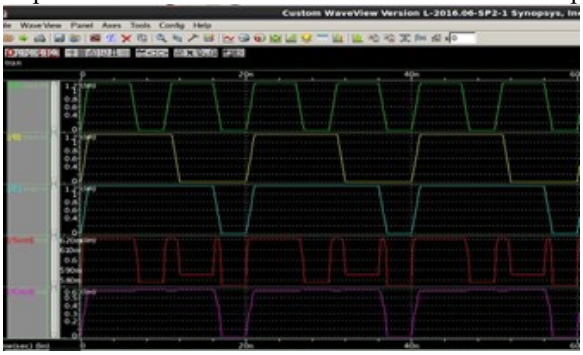


Fig 6: Output Waveform of Conventional 10T Fast data computation



VII. CONCLUSION

Fast data computation benchmark circuits employing two-input NANDs and NORs, inverters, and flip-flops verified the suggested methodology. We also took into consideration XNORs and two-input XORs. The acquired results were assessed using various cost functions, including area, power, performance, inverter and transistor counts, and so on. The suggested method demonstrates its value when compared to cutting-edge algorithms for technologically rapid data computation. We may concurrently lower the average number of inverters, transistors, area, power dissipation, and latency by up to 48%, 5%, 5%, 5%, and 53%, respectively, when compared to academic and commercial methodologies. Using a coarse-grained, program-level parallel method, the suggested AIG node count minimization can be completed more quickly.approach. To expedite this optimization process, all five minimization approaches can be executed in simultaneously, as opposed to one serial operation. In the event of temporal constraints in synthesis, a conventional cell with varying drive intensities might also be employed, allowing a gate sizing step to manage the required trade-off. 86 In conclusion, wire delay is becoming more relevant than cell delay in advanced technology, especially for long wires, and position and route can have a big impact on circuit performance. Our goal is to utilize this basic cell-based method in a logic synthesis environment that takes physical considerations into account. This approach has already been the subject of experiments (MATOS; REIS, 2015; MATOS et al., 2015b), and we have also suggested a novel method to bring technology information Particularly associated with location and path, these pertain to the initial phases of logic synthesis (REIS; MATOS, 2017). However, the current findings have demonstrated the computational and practical feasibility of the approaches described here, even though the research presented paved the way for a number of subsequent studies. The suggested algorithms have shown to be beneficial for effectively quick data computation VLSI circuits built using basic cells. The majority of VLSI applications limited to basic cells mentioned in this study can benefit from the suggested approaches.

REFERENCES

[1] K. Pagiamtzis and A. Sheikholeslami, “Static RAM memory (XNOR-XOR) circuits and architectures: A tutorial and survey,” IEEE J. Solid-State Circuits, vol. 41, no. 3, pp. 712–727, Mar. 2006.

[2] S. Hanzawa, T. Sakata, K. Kajigaya, R. Takemura, and T. Kawahara, “A large-scale and low-power XNOR-XOR architecture featuring a one-hot-spot block code for IP- lookup in a network router,” IEEE J. Solid-State Circuits, vol. 40, no. 4, pp. 853–861, Apr. 2005.

[3] C.Nagarajan and M.Madheswaran - ‘Experimental verification and stability state space analysis of CLL-T Series Parallel Resonant Converter’ - Journal of ELECTRICAL ENGINEERING, Vol.63 (6), pp.365-372, Dec.2012.

[4] C.Nagarajan and M.Madheswaran - ‘Performance Analysis of LCL-T Resonant Converter with Fuzzy/PID Using State Space Analysis’- Springer, Electrical Engineering, Vol.93 (3), pp.167-178, September 2011.

[5] C.Nagarajan and M.Madheswaran - ‘Stability Analysis of Series Parallel Resonant Converter with Fuzzy Logic Controller Using State Space Techniques’- Taylor & Francis, Electric Power Components and Systems, Vol.39 (8), pp.780-793, May 2011.

[6] C.Nagarajan and M.Madheswaran - ‘Experimental Study and steady state stability analysis of CLL-T Series Parallel Resonant Converter with Fuzzy controller using State Space Analysis’- Iranian Journal of Electrical & Electronic Engineering, Vol.8 (3), pp.259-267, September 2012.

[7] Nagarajan C., Neelakrishnan G., Akila P., Fathima U., Sneha S. “Performance Analysis and Implementation of 89C51 Controller Based Solar Tracking System with Boost Converter” Journal of VLSI Design Tools & Technology. 2022; 12(2): 34–41p.

[8] C. Nagarajan, G.Neelakrishnan, R. Janani, S.Maithili, G. Ramya “Investigation on Fault Analysis for Power Transformers Using Adaptive Differential Relay” Asian Journal of Electrical Science, Vol.11 No.1, pp: 1-8, 2022.

[9] G.Neelakrishnan, K.Anandhakumar, A.Prathap, S.Prakash “Performance Estimation of cascaded h-bridge MLI for HEV using SVPWM” Suraj Punj Journal for Multidisciplinary Research, 2021, Volume 11, Issue 4, pp:750-756

[10] G.Neelakrishnan, S.N.Pruthika, P.T.Shalini, S.Soniya, “Perfromance Investigation of T-Source Inverter fed with Solar Cell” Suraj Punj Journal for Multidisciplinary Research, 2021, Volume 11, Issue 4, pp:744-749

[11] C.Nagarajan and M.Madheswaran, “Analysis and Simulation of LCL Series Resonant Full Bridge Converter Using PWM Technique with Load Independent Operation” has been presented in ICTES’08, a IEEE / IET International Conference organized by M.G.R.University, Chennai.Vol.no.1, pp.190-195, Dec.2007

[12] M Suganthi, N Ramesh, “Treatment of water using natural zeolite as membrane filter”, Journal of Environmental Protection and Ecology, Volume 23, Issue 2, pp: 520-530,2022

[13] M Suganthi, N Ramesh, CT Sivakumar, K Vidhya, “Physiochemical Analysis of Ground Water used for Domestic needs in the Area of Perundurai in Erode District”, International Research Journal of Multidisciplinary Technovation, pp: 630-635, 2019

[14] Arsovski and A. Sheikholeslami, “A mismatch-dependent power allocation technique for match-line sensing in Static RAM memories,” IEEE J. Solid-State Circuits, vol. 38, no. 11, pp. 1958–1966, Nov. 2003.

[15] K. Pagiamtzis and A. Sheikholeslami, “A low-power Static RAM memory (XNOR-XOR) using pipelined hierarchical search scheme,” IEEE J. Solid-State Circuits, vol. 39, no. 9, pp. 1512–1519, Sep. 2004.