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Cooperative Spectrum Sensing Architecture For Energy Efficient Data-Fusion Based Cognitive Radio Network

Dr. S. Sankar ganesh
Associate Professor
Department of VLSI, AVS Engineering College, Salem.

G. Prekeshwari
PG Student
Department of VLSI, AVS Engineering College, Salem.

Abstract - The use of available radio frequency bands has become more demanding, and Cognitive Radio (CR) technology has emerged as a possible way to meet this requirement. In order to facilitate data fusion in cooperative cognitive radio networks, a unique hardware-efficient Spectrum-Sensor Very Large-Scale Integration (VLSI) architecture is proposed in this research. The suggested design uses a collaborative strategy that makes use of data fusion techniques to address the difficulties associated with spectrum sensing and management. Our VLSI architecture optimises resource utilisation while retaining high performance by fusing cutting-edge sensing algorithms with effective hardware design. The cognitive-radio network's cooperative structure increases overall spectral efficiency and improves spectrum awareness.

In order to empower the network to make defensible decisions based on the aggregate information obtained from dispersed spectrum sensors, the study investigates the integration of data fusion approaches. The suggested architecture's hardware efficiency, low power consumption, and real-time flexibility to changing spectrum conditions are its salient characteristics. Through simulations and comparisons with current solutions, the system's efficacy is assessed, showcasing higher performance in terms of spectrum sensing speed and accuracy. The results of this project are important for developing next-generation communication systems and implementing effective paradigms for spectrum sharing.

Key Words:Cognitive radio (CR), Cooperative Cognitive Radio Networks (CCRN), Cooperative Spectrum Sensing (CSS),Orthogonal Frequency Division Multiplexing (OFDM), Very Large-Scale Integration (VLSI) algorithm.

I. INTRODUCTION

As the demand for data increases, there is a growing congestion of the radio spectrum, which is an essential resource for wireless communication. In response to this issue, cognitive radio (CR) technology appears, which allows unlicensed users (also known as secondary users) to opportunistically access spectrum areas that primary users aren't using. However, accurately identifying these empty bands is necessary for effective spectrum utilisation, which presents a substantial problem. Due to fading channels and noise, traditional spectrum sensing by individual secondary users frequently has poor detection accuracy. A viable answer is provided by cooperative spectrum sensing (CSS) initiatives. CSS maximises spectrum utilisation and enhances detection accuracy by combining data from several secondary users. But putting CSS into practice requires effective data processing and user communication.

This is where cooperative spectrum sensors (CSRs) with hardware-efficient VLSI architectures come into play. Miniaturisation and optimised data flow are made possible by VLSI technology, which is essential for real-time spectrum sensing in resource-constrained CR networks. In particular, this work provides a unique hardware-efficient VLSI architecture for a CSR intended for cooperative cognitive radio networks based on data fusion. Our architecture uses a data-fusion-based algorithm to overcome the drawbacks of previous systems. We minimise computation complexity and maximise detection accuracy by leveraging effective fusion techniques to combine data from many users.

1.1 PROBLEMSTATEMENT:

The computational complexity of traditional CSS methods makes them difficult to execute on devices with limited resources. It's possible that current VLSI architectures for spectrum sensors are overly dependent on hardware or aren't optimised for data fusion.

Considering this as a problem, a hardware-friendly data fusion approach that reduces computing complexity without sacrificing good spectrum sensing performance has been developed. For the Data Fusion Centre, create a VLSI architecture that is efficient in terms of space, power, and processing performance. The selected data fusion algorithm should be optimised for this architecture.

1.2 OBJECTIVE:

This paper's primary goal is to create a VLSI architecture that opens the door for tiny, low-power cognitive radio devices with dependable spectrum sensing in CCRN

II. LIERATURESURVEY:

[1] It suggests a new digital architecture for a spectrum sensor based on maximum-minimum-eigenvalue (MME) that has a reduced critical-path delay and a shorter sensing time. To further improve hardware efficiency, this architecture has shared resources. Our MME spectrum sensor has undergone hardware development on an FPGA platform, and real-time testing is done in a communication context. We created and replicated the suggested digital sensor using a 90 nm-CMOS technology, yielding an area of 0.42 mm2. It

functions at a maximum clock frequency of 404 MHz, resulting in a sensing time of 53.5 µs

[2] New VLSI architectures based on suggested spectrum sensing algorithms have been presented in this work. We present two types of sensor architectures: (1) memory-less & low-latency (2) memory-based & resource-shared spectrum-sensor architectures. Performance analyses of suggested MED, MSEE and EME spectrum sensing algorithms in AWGN environment showed that the detection probability of 0.75 could be achieved at the SNRs of -12 dB, -10 dB and -7 dB respectively.

[3] An area-efficient method for cooperative spectrum sensing (CSS) in a cognitive radio network based on data fusion is presented in this brief. It can accurately identify the prime user's spectrum occupancy by combining the signals received from six subordinate users.

[4] It suggests a novel selective-sampling method for modern cognitive-radio wireless networks that permits spectrum sensing of OFDM primary users with 64, 128, 256, 512, and 1024 subcarriers. The time domain cyclostationary detector's reconfigurable and memory-efficient VLSI architecture was created for spectrum sensing.

[5] It is possible for many algorithms to temporally and spatially share the FPGA resources, which could result in resource underutilization or reconfiguration overhead. FCNNLib to manage several convolution algorithms on FPGAs with varying latency and throughput trade-offs.

2. BLOCKDIAGRAM:

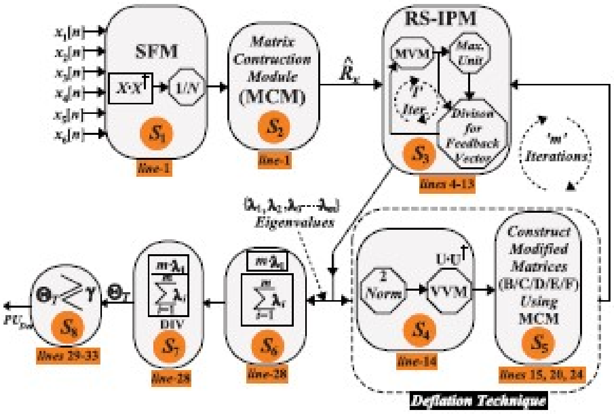


Fig-3:Design of proposed CSR architecture based on the suggested CSS algorithm

2.1 DESCRIPTION:

Joint Power and Subcarrier Allocation for Throughput Maximization:

The optimisation problem can be reduced to the problem of jointly assigning subcarriers and power among all users in the network to achieve the maximum overall throughput, given the ideal power division scheme between eNB and RS for each subcarrier. The simplified issue can be expressed as:

$$\sum_{k \in M, l \in N} R^{(k,l)}$$

The joint subchannel and power allocation scheme in terms of maximizing the overall throughput is concluded in Algorithm 1 is defined as:

$$(x)^+ = \{x, x \geq 0, 0, x < 0.$$

It has proved that assigning exclusively one user with the best channel quality to every subchannel is optimal by induction.

Joint Power and Subchannel Allocation with Fairness Concern:

The two goals are arranged hierarchically, with the fairness goal being the most important to optimise and the overall throughput being further maximised among workable solutions. We employ the fairness definition, according to which having the same data rate for every user achieves maximal fairness. By maximising the poorest user's achievable rate through the solution of the max-min problem, the maximum fairness can be achieved.

$$R_K - \sum_{l \in N} \frac{\rho^{(K,l)}}{n} \log\log\left(1 + H^{(K,l)} p^{(K,l)}\right)$$

Optimal Power and Subchannel Allocation:

The following theorem describes a sufficient condition that the optimal joint power and subchannel allocation meets in order to solve this lexicographic maximisation problem. Regardless of subchannel assignment, water-filling power allocation is always the best option, hence power allocation should still follow this strategy to maximise throughput overall. Assume that the channel gains on each subchannel determine the water filling level, λ. The achievable rate for user k can be derived as follows:

$$R_K = \frac{1}{n} \log\log\left(H^{(S_k^+)} \lambda^{(S_k^+)}\right)$$

Thus, if$H(S_k^+)\lambda(S_k^+)$ is balanced to produce the same value for every user $k \in M$, that is the optimal scenario. However, because to the computational complexity, it is very difficult to jointly distribute subchannels and power, since λ is a function of all channel gains, which will be decided by the subchannel assignment. Rather, the joint allocation is divided into two parts by the majority of unsatisfactory solutions to the comparable problem. Subchannels are first assigned with the assumption that transmission power is dispersed equally among all subchannels. After that, power distribution is optimised in accordance with water-filling based on the subchannel allocation.

Suboptimal Power and Subchannel Allocation

There are two steps in the suboptimal resource allocation system as well. First, we distribute subchannels among all users under the assumption that powers are distributed with a water-filling level of λ. Subchannel allocation in the first phase can then be used to determine λ in the second step.

1) Suboptimal Subchannel Allocation Algorithm:

The subchannel allocation mechanism is the sole topic of the first stage. Two new sets are introduced first, and then the subchannel allocation mechanism is suggested. Assume that after allocation, $N_s$is the subchannel set that remains. Initially, $N_s = N$. Define M_s as an ordered set containing all users 1, 2, . .,m where for any $i, j \in M_s$, $i < j$ if and only if $H(S_i) \leq H(S_j)$.

Suboptimal subchannel allocation algorithm
1: Initialize: $S_k = \Phi$, $H(S_k) = 1$ for all users k = 1,2,…..,m. Let $N_s = N$ and $M_s = M$.
2: While $N_s \neq \Phi$, for $M_s(1)$,…..,$M_s(m)$, find a sub-channel $l(k)$ ε N_s satisfying $H^{(k,l(k))} >= H^{(k,l')}$ for all l' ε N_s. Assign l(k) to user k. Update $N_s = N_s - \{l(k)\}$ and $H^{(S_k)} = H^{(S_k)} \cdot H^{(k,l(k))}$
3: Reorder the user set Ms. Then go back to 2.

2) Optimal Power Allocation:

Assume that each subchannel has a channel gain coefficient of$H^{(k,l)}$after the subchannels have been allocated based on the algorithm. As per the ideal distribution of water-filling power, the power allotted to every subchannel equals

$$P^{(k,l)} = \left(\lambda - \frac{1}{H^{(k,l)}}\right)^+$$

and λ is chosen to satisfy _ the total power constraint

$$\sum \quad P^{(k,l)} = P_{total}.$$

MIMO Process:

Multiple-Input Multiple-Output (MIMO) is one of several forms of multiple antenna techniques available today designed to significantly improve communication performance. In wireless communications, where devices operate in high multipath conditions, MIMO is particularly appealing because to its potential to enhance data rates while maintaining spectral efficiency. As a result, it has recently been adopted or is being considered for usage by wireless protocols such as WLAN 802.11n, IEEE 802.16 (adopted by the Wi MAX™ Forum), and 3GPP Long Term Evolution (LTE). It is anticipated that all future 4G wireless communication systems would make use of MIMO technology.

Spatial diversity, spatial multiplexing, and beam shaping are the three general categories of multiple antenna approaches. Spatial multiplexing is utilised by MIMO systems. To boost the effective data rate in rich scattering situations, separate data streams are simultaneously sent over various antennas. A minimum of two transmitters and two receivers are needed for MIMO spatial multiplexing, and the receivers must be located in the same location (i.e., same device). Two mobiles can be used together for MIMO in the uplink since the transmitters do not need to be in the same device. In this instance, the base station must synchronise the transmissions, which entails aligning the time and power level of the mobile devices. This is a necessary step for regular cellular operation.

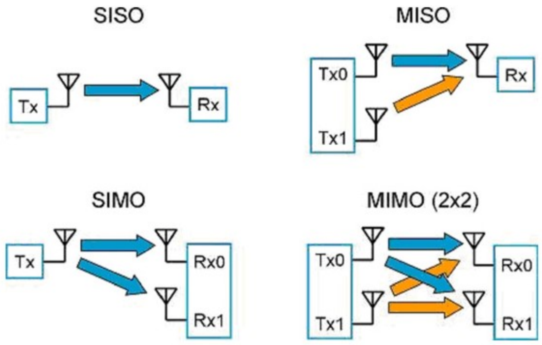


Fig-3.1 This graphic depicts antenna and channel configurations for SISO, SIMO, MISO, and MIMO (2x2) systems.

There are two antennas at the transmitter, each of which has two distinct transmit channels, and two antennas at the receiver, each of which has two distinct receive channels. There are also a plethora of more MIMO configurations that may be achieved by combining numerous antenna pairs, including 3x3 and 4x4. Even an uneven number of antennas at the transmitter and receiver, or aMxN scenario where M transmit antennas and N receive antennas are not equal, can be configured for a MIMO system.

III. WORKING:

Cooperative MIMO, also known as network MIMO, distributed MIMO, virtual MIMO, or virtual antenna arrays, is a wireless communication technology that leverages the spatial diversity of multiple radio devices to achieve performance with distributed antennas.

The stream of data to be transferred is divided into several parts. Then, every stream is sent out from a distinct virtual array device. The transmitted signals experience various fading circumstances as a result of the devices' spatial separation from one another, which increases signal variety and lessens the effects of signal interference. To retrieve the original data, all of the devices' received signals are merged and processed together at the receiver side.

Cognitive Radio Networks (CRNs):These are wireless networks that enable gadgets to detect radio frequencies and take advantage of underutilized ones. This makes it possible to use the spectrum more effectively than with typical static allocation.

Cooperative Spectrum Sensing (CSS):Multiple cognitive radios can work together in CRNs to increase spectrum sensing accuracy. This is because certain radios may have restricted detecting power because of things like obstructions or noise.

Data Fusion:This is the procedure for fusing data from several sources to get a more precise image. To ascertain spectrum availability in CSS, sensor data from many cognitive radios is combined using data fusion techniques.

VLSI Architecture:The design of integrated circuits (ICs) with an extremely high transistor density is referred to here. Here, creating an efficient hardware architecture for the spectrum sensor in terms of both power consumption and area usage is the main goal.

Overall, this research could lead to more efficient and reliable spectrum sensing in CRNs, enabling better utilization of the radio spectrum.

3. DESIGN FLOW IN VLSI:

Thebelowshowsthedesign flow for Verilog HDL in Xilinx ISE Design,

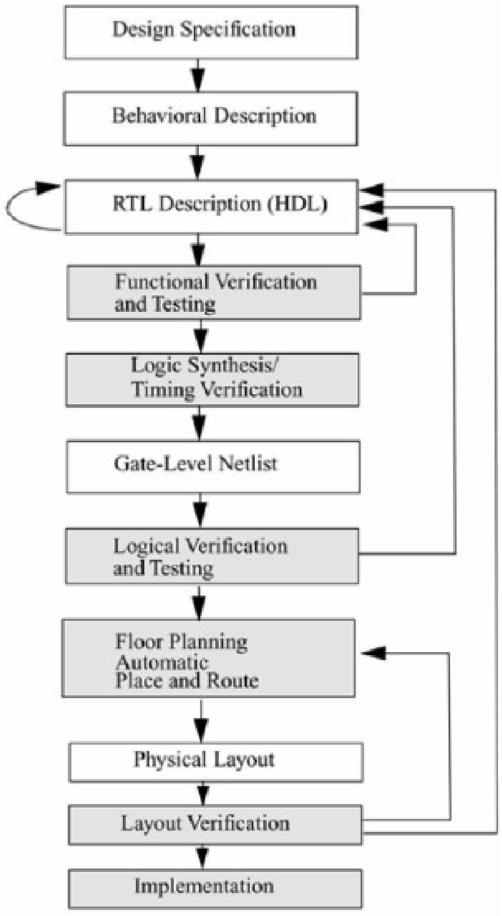


Fig-5:Design Flow

IV. RESULTS AND CONCLUSION:

Cognitive radio is a kind of wireless communication in which gadgets may scan the radio spectrum for unoccupied frequencies. As a result, they can live in harmony with authorised users without creating any problems. This paper focuses on the cooperative cognitive radio networks' data fusion component. Several radios operate together in these networks to increase the precision of spectrum sensing. This design puts reduced area and power consumption first while yet performing well in terms of identifying underutilised frequencies.

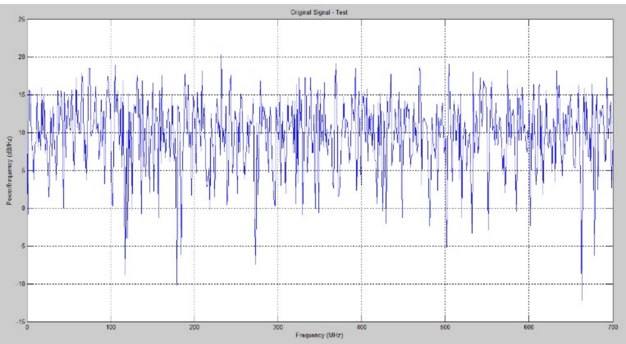


Fig-6.1:Original Signal Test

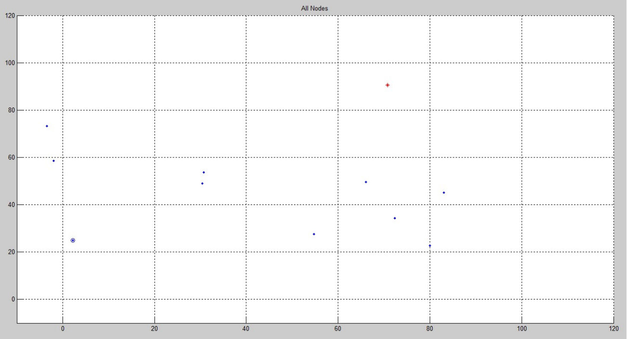
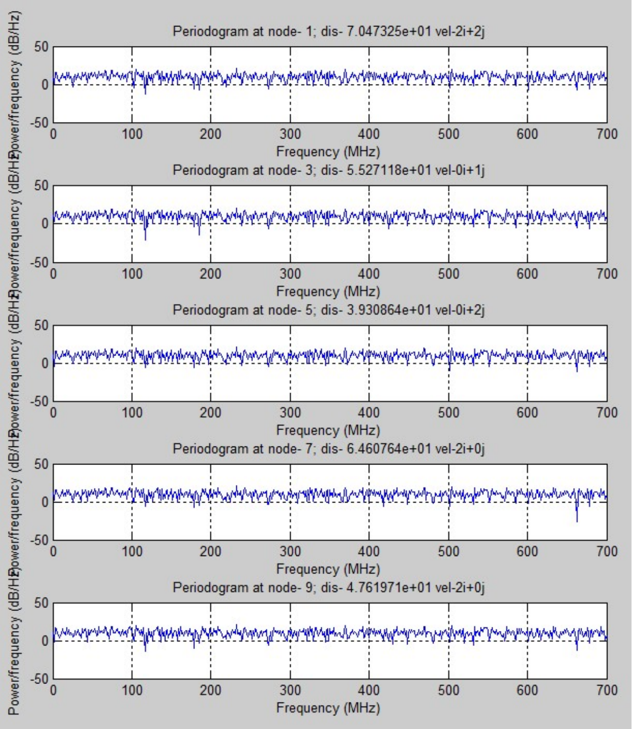


Fig-6.2:Multiple Nodes (Signal Towers)

Fig-6.3:Periodogram for odd nodes



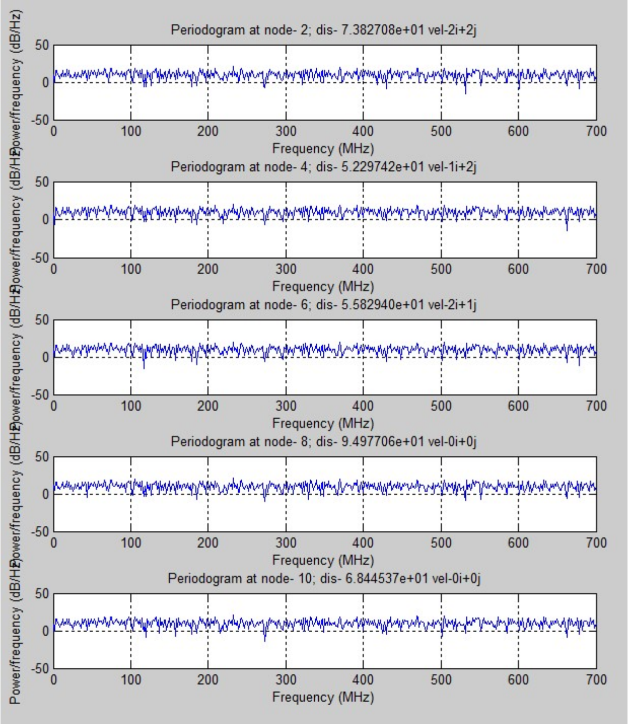
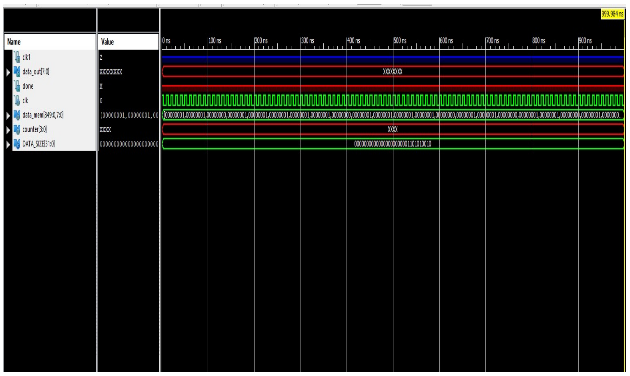


Fig-6.4:Periodogram for even nodes

Fig-6.5:CCRN Data signal



Name	Value
clk1	Z
data_out[7:0]	XXXXXXXX
done	X
clk	0
data_mem[849:0,7:0]	{00000001,00000001,00
counter[3:0]	XXXX
DATA_SIZE[31:0]	0000000000000000000000

V. FUTURESCOPE:

This architecture for spectrum sensing in cognitive radio networks holds promise for several future advancements:

- Increased Network Size:There are only so many secondary users that the existing design can accommodate. In the future, the architecture might be scaled to support a bigger network, allowing for more effective spectrum utilisation.
- Enhanced Data Fusion Algorithms:The architecture is dependent on a particular method of data fusion. Subsequent investigations may investigate the integration of more advanced algorithms to enhance spectrum sensing precision while preserving hardware effectiveness.
- Integration with Reconfigurable Hardware:Introducing adaptability could be achieved by combining this VLSI architecture with reconfigurable hardware, such as FPGAs. This would enable the system to adapt without requiring a total redesign to various sensing conditions.

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