Optimizing Lookup Tables for CRC based Multiple Error Correction

M.Shanmugam[1]
Assistant Professor
Department of Electronics and Communication Engineering,
Mahendra Engineering College, Namakkal, Tamilnadu, India.

J.Pavithra[2], P.Priyadharshini[3], V.Saran[4], G.Vijayalakshmi[5]
Department of Electronics and Communication Engineering,
Mahendra Engineering College, Namakkal, Tamilnadu, India.

Abstract- Present energy-efficient error control code maximum bit error correction technique that can correct any type of error pattern including random errors, burst errors, and a combination of random and burst errors that count up to five and simultaneously avoid crosstalk. Error correction codes (ECC) are widely used to ensure data integrity and reliability in various digital communication systems. One common ECC technique is Cyclic Redundancy Check (CRC), which detects errors by appending a checksum to the data stream. To overcome this limitation, the concept of CRC-based multiple errorcorrection has been introduced. CRC-based multiple error correction utilizes alookup table, also known as a syndrome table, to map the syndrome generatedby the CRC algorithm to the corresponding error patterns. The primary objective is to reduce the table's size while maintaining its effectiveness in correcting errors.

Initially, the CRC algorithm is used on a set of error patternsto generate syndromes. These syndromes are analyzed to identify any patterns or repetitions that can be exploited for compression. By identifying and compressing similar syndromes, the size of the lookup table can be significantly reduced. Furthermore, error patterns that lead to the same syndrome are consolidated to eliminate redundant entries in the lookup table. The performance of the system in terms of error detection and correctioncapabilities is evaluated and compared against traditional CRC and other existing multiple error correction techniques. Overall, these abstract highlights the importance of optimizing the lookup table for CRC-based multiple error correction. The findings of this research provide insights into improving the error correction capabilities of CRC-based systems, thereby enhancing the reliability of digital communication systems.

I.INTRODUCTION

With the shrinking feature size and increasing die size, the integration of a large numberof functional blocks, storage elements, and intellectual property (IP) in a single chip increase. As the number of functional blocks in a single chip increase, the bus-based. Communication becomes inefficient in a system-on-chip (SOC). Networks-on-chip (NOC)is a paradigm that provides a solution to the communication problem in a SOC. In NOC, the functional blocks communicate through routers. Routers are interconnected using interconnection wires.

In nano-scale technology, due to scaling of supply voltage, increasing interconnectdensity, and faster clock rates, on-chip interconnect wires suffer from three major problems. They are (i) delay; (ii) power consumption; and (iii) reliability.

The probability of adjacent multi-wire (burst error) errors is much higher than the probability of multiple random multi-wire (random) errors. Hence detection and correctionof random as well as burst error is important to increase the reliability of the NOC interconnect. Thus to have a good performance in the design of a chip interconnection network, delay, power, and reliability are the three major issues to be addressed. Low-powercoding techniques have been proposed to reduce the power consumption of the interconnection wire by reducing the switching activity in the interconnection wires. Crosstalk avoidance codes (CACS) are proposed to reduce the delay problem. To increase the reliability, error control codes such as automatic repeat request (AEQ), hybrid ARQ (HARQ), and forward error correction (FEC) have been proposed. Joint crosstalk avoidance and forward error correction schemes have been proposed to address the delay and reliability problems. These techniques avoid crosstalk and correct any error patterns of up to three errors only. In the correct up to 4-bit errors without using crosstalk avoidance code. In this paper, to address the delay and reliability problem of the NOC interconnect link, we propose combined random and burst error correction code with crosstalk avoidance. The proposed code power dissipation has become a critical design criterion in most system designs, especially in portable battery-driven applications such asmobile phones, pads, laptops, etc.

Therefore, various techniques have been proposed in the literature, which encode the data before transmission on the off-chip buses to reduce the average and peak number of transitions. Since the instruction addresses are mostly sequential, gray coding was proposedto minimize the transitions on the instruction address bus.

The gray code ensures that when the data is sequential, there is only one transitionbetween two consecutive data words. However, this coding scheme may not work for data address buses because the data addresses are typically not sequential. An encoding scheme called t0 coding was proposed for the instruction address bus. This coding uses an extra bitline, an increment bit-line along with the address bus, which is set when the addresses on the bus are sequential, in which case the data on the address bus is not altered. When the addresses are not sequential, the actual address is put on the address bus. Bus-invert (bi) coding is proposed for reducing the number of transitions on a bus.

In this scheme, before the data is put on the bus, the number of transitions that mightoccur with respect to the previously transmitted data is computed. If the transition count ismore than half the bus width, the data is inverted and put on the bus. An extra bit line is used to signal the inversion on the bus. Described a generic encoder-decoder architecture, which can be customized to obtain an entire class of coding schemesfor reducing transitions. The same authors proposed ICC-XOR coding, which reduces thetransitions on the instruction address bus better than any other existing technique. An adaptive encoding method is also proposed. But with huge hardware overhead.This scheme uses a RAM to keep track of the input data probabilities, which are used to codethe data. Another adaptive encoding scheme is proposed which does encoding based on theanalysis of previous n data samples. This again has a huge computational overhead. Propose a working zone encoding (WZE) technique, which works on the principle of locality. Although this technique gives good results for data address buses, there is a huge delay and hardware overhead involved in encoding and decoding.

Moreover, this technique requires extra bit lines leading to redundancy in space theexisting methods give significant improvement on instruction address buses, but none of the encoding methods gives any significant improvement on the data and multiplexed address buses consistently without redundancy in space or time. This is because most of the proposed techniques are based on the heuristic that the addresses on the bus are sequentialmost of the time. On data address buses, the addresses are not sequential, and hence the existing techniques fail to reduce transition activity.

In this system, the design of high-speed and energy-efficient transceivers for global interconnects of network-on-chips (NOCS) has become an active field of research over the last decade. The throughput and the performance of multiprocessor systems on chips (MPSOCS) are dependent on the speed of data communication across the global interconnects. The progress of fabrication technology has decreased the device dimensions and hence increased the speed of the processors in the MPSOCS.

The shrinkage of the device size has also led to the integration of more processors on the same die. However, the inclusion of multiple processors has made the die size larger, and as a result, the length of the global interconnects connecting them is becoming longer. The long global interconnects not only take the significant area of the highermetal layers. These parasitic affect the speed of data links and cause significant power loss,particularly for high-speed data Communication.

Several techniques have been proposed in order to tackle these problems of speed and power for high-speed data transmission across long unrepeated interconnects.For transmitting n-streams of high-speed data using differential signaling, the totalnumber of signal lines required is 2n. The number increases to 3n if shielding ground linesare introduced in between two differential pairs to reduce the crosstalk, so the corresponding wire efficiency is 33%. Various schemes have been adopted for increasing the wire efficiency for on-chip signaling. For example, an optimum twist technique reduces the crosstalk and hence eliminates the need to shield the differential lines, and thereby, the wiring efficiency becomes 50%. To further improve the efficiency to 100%, has used single-ended communication. It has proposed a receiver to eliminate the far-end crosstalk caused by adjacent interconnects.

An NOC architecture has been proposed, where serves has been used to decrease the interconnect area. However, serialization increases the bandwidth requirement of the link keeping the wire efficiency unchanged. A coded differential signaling scheme has been proposed for off-chip communication to increase the wire efficiency. In this technique, the signal wires carry multiple levels in contrast to two levels in non-return-to-zero differential signaling. These techniques are immune to common mode noise like conventional differential signaling and also reduce the simultaneous switching noises of the nearby interconnects. Such techniques can be adapted to increase the wiring efficiency in on-chip links. However, these architectures use resistive termination followed by a voltage mode receiver to retrieve the signals.

This system is proposed for combined crosstalk avoidance and error correction code and has focused only on correcting errors of a maximum ofthree bits. The worksproposed use a dap coding scheme and correct only one, two, or three-bit errors with crosstalk avoidance. However, the work proposed in this paper corrects any error pattern up to five including a combination of random and burst errors and simultaneously avoiding crosstalk between interconnect wires. This is the first error correction code proposed with crosstalk avoidance to correct any error

pattern of up to five for on-chip interconnect links. The proposed error control code is named a multi-bit random and burst error correction code with crosstalk avoidance.

II.AIM OF THE PROJECT

- Transferring data between two points is essential, also the accuracy of the transferred data is vital for some critical applications, but an error during the transmission of data is very common.
- The Cyclic Redundancy Check (CRC) method is generally used for error detection and correction. In this system, we have proposed a new technique for error detection and correction in the case of CRC-16, which is hardware-optimized and works at relatively higher frequency and speed.
- In the proposed method, it is possible to detect the exact place of single bit errors and correct them using minimum hardware.
- This method involves no look tables and hence is memory efficient codes that correct errors are essential to modern civilization and are used in devices from modems to planetary satellites.
- The theory is mature, difficult, and mathematically oriented, with tens of thousands of scholarly papers and books, but this project will describe only a simple and elegant code,discovered in 1949.

III.LITERATURE REVIEW

3.1 CRC-Based Correction of Multiple Errors Using an Optimized Lookup Table, VIVIENBOUSSARD, STEPHENECOULOMBE, FRANCISXAVIERCOUDOUX, PATRICK CORLAY,2022.

ABSTRACT

In this paper, propose an optimized table-based method for performing multiple error correction based on the CRC syndrome. The approach offers a low-complexity alternative to the state-of-the-art error correction method as it generates a table that containsprecomputed operations required to perform error pattern searches, avoiding most to all arithmetic operations. Thanks to offline table generation, the proposed approach achieves the same error correction performance as state-of-the-art approaches while providing computational savings and thus improving processing speeds. Since this greatly increases the number of candidates in the output error pattern list, present a validation step, that increases the correction rate for lists containing many candidates. Other validation steps could be used such as those based on bit error probability. Future work will look at integrating the proposed CRC-based error correction solution into a complete cross-layer receiver architecture to benefit from other validation mechanisms available in theprotocol stack. The objective is to further reduce the list size or to be able to determine thebest candidate out of several to reconstruct the best signal quality at the receiver side (e.g., visual quality, in the case of video content transmission).

METHODOLOGY

In this paper, propose a new approach to perform multiple error corrections in wireless communications over error-prone networks. It is based on the cyclic redundancy check syndrome, using an optimized lookup table that avoids performing.

This method can achieve the same correction performance as the state-of-the-art approaches while significantly reducing the computational complexity. The table is designed to allow multiple-bit error correction simply by navigating within it. Its size is constant when considering more than two errors, which represents a tremendous advantage over earlier lookup table-based approaches. Simulation results of a C implementation performed on a Raspberry Pi 4 show that the proposed method can process single anddouble error corrections of large payloads in 100 ns and 642µs, respectively. At the same time, it wouldtake 300µs and 1.5 s, respectively, with the state-of-the-art CRC multiple error correction technique.

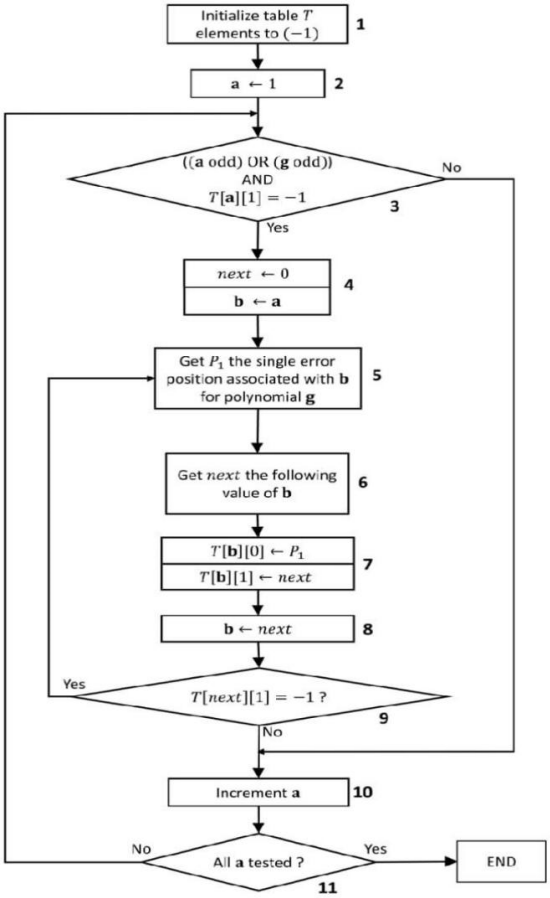

Fig 3.1.1 Flowchart representation of the steps to generate table T containingsingle error position and the next element to handle double error corrections

CONCLUSION

This represents a speedup of nearly 3000× for single error and 2300× for double error correction, respectively. Compared to table-based approaches, the proposed method offers a speedup of nearly 1200× for single error and 2300× for double error correction under the same conditions. also show that when multiple candidate error patterns are present, numerous errors can be corrected by adding a checksum cross-validation step.

IV.PROPOSED METHOD

The proposed maximum bit error correction technique encoder uses SEC–DED extended cyclic redundancy check code (39,32) to encode the initial message bits. The triplication error correction scheme is one of the standard error correction schemes used in communication systems to correct errors. We propose a triplication error correction scheme to correct the errors in the on-chip interconnection link. Using a triplication error correction scheme, each of the encoded message bits is triplicated. Thus if the initial SEC–DED extended cyclic redundancy check code is (n,l), where n is the encoded message andl is the original message, then the final number of bits in the triplication message is 3n.

The triplication of the message bit is used to correct the errors and simultaneously avoids crosstalk. The triplication of the encoded message increases the minimum cyclic redundancy check distance to 12. Based on information coding theory, the minimum cyclicredundancy check distance of k can correct bit 1þ=2c errors. Therefore, the maximum bit errorcorrection technique code can correct up to five errors. The block diagram of the proposed maximum bit error correction technique encoder is shown in Fig And the flow diagram is shown in Fig. The general algorithm generates a single-error correcting (SEC) code for anynumber of bits.

Modalism is a verification and simulation tool for VHDL, Verilog, system Verilog, and mixed language designs. This lesson provides a brief conceptual overview of the modalism simulation environment. Modalism uses libraries in two ways: 1) as a local working library that contains the compiled version of your design; and 2) as a

resource library. Modalism offers numerous tools for debugging and analyzing your design. Several of these tools are covered in subsequent lessons, including using projects, working with multiple libraries, setting breakpoints and stepping through the source code, viewing waveforms and measuring time, viewing and initializing memories, creating stimulus with the waveform editor, and automating simulation. The Modalism library format is compatible across all supported platforms.

Triplication error correction is a scheme used to optimize the look-up table for CRC-based multiple error correction. In this scheme, three replicas of the look-up table are stored, and error correction is performed using a voting mechanism. In CRC-based multiple error correction, a look-up table is used to determine the correct bits in the received message. This table stores precomputed syndrome values (check values) for all possible error patterns. Each syndrome value corresponds to a specific error pattern, and by comparing the received syndrome value with the precomputed values, the errors can be identified and corrected. Optimizing the look-up table is crucial for efficient error correction. One way to achieve this is by using a triplication error correction scheme. In this scheme, three replicas of the look-up table are stored, known as replica A, replica B, and replica C. During the error correction process, each replica of the look-up table is accessed independently. The received syndrome value is compared with the values stored in each replica. If two replicas agree on a particular syndrome value, it is considered the correct value. However, if there is a disagreement among the replicas, a voting mechanism is used to determine the correct syndrome value.

In the world of data transmission and storage, error correction is a crucial aspect to ensure the accuracy and integrity of the transmitted or stored information. One widely used error correction scheme is the triplication error correction scheme. The triplication error correction scheme, as the name suggests, involves duplicating the original data three times. This redundancy allows for the detection and correction of errors that may have occurred during transmission or storage. Let's take a closer look at how this scheme works. In the triplication scheme, the original data is divided into three identical copies, each of which is transmitted or stored independently. These copies are typically referred to as Triplicate A, Triplicate B, and Triplicate C. During transmission, the three copies are sent separately to their respective destinations. This helps mitigate the impact of errors that may occur during the transmission process. If one of the triplicates gets corrupted, the other two can be used to detect and correct the error.

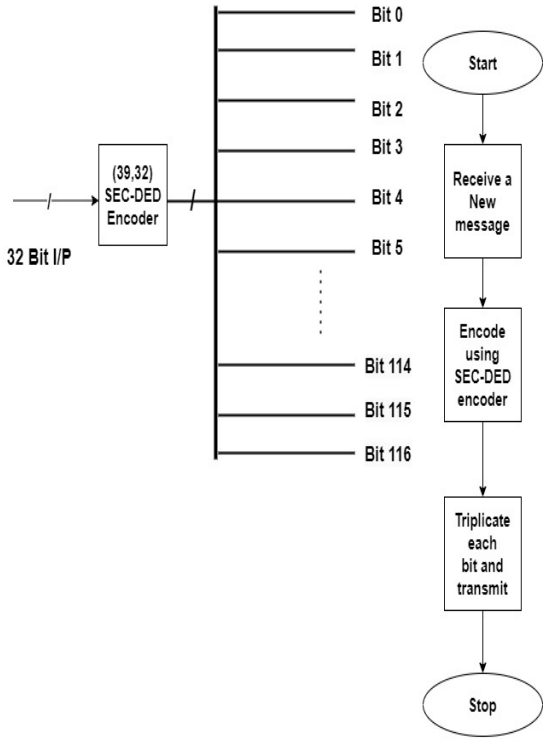

Fig 4.2.1 Proposed maximum bit error correction technique decoder

V.CONCLUSION

The proposed maximum bit error correction technique encoder uses SEC-DED extended cyclic redundancy check code (39,32) to encode the initial message bits. The triplication error correction scheme is one of the standard error correction schemes used in communication systems to correct errors. Propose a triplication error correction scheme to correct the errors in the on-chip inter-connection link. Using a triplication error correction scheme, each of the encoded message bits is triplicated. Thus if the initial SEC_DED extended cyclic redundancy check code is (N, l), where n is the encoded message and l isthe original message, then the final number of bits in the triplication message is 3n. The triplication of the message bit is used to correct the errors and simultaneously avoids crosstalk.

REFERENCES

[1] r. Ho et al., "High speed and low energy capacitively driven on-chip wires," ieee j. Solid-state circuits, vol. 43, no. 1, pp. 52–60, Jan. 2008.

[2] e. Men sink, d. Schinkel, e. A. M. Klumperink, e. Van tuijl, and b. Nauta, "power efficient gigabit communication over capacitively driven rc-limited on-chip interconnects," ieee j. Solid- state circuits, vol. 45, no. 2, pp. 447–457, Feb. 2010.

[3] r. Ho et al., "high speed and low energy capacitively driven on-chip wires," ieee j. Solid-state circuits, vol. 43, no. 1, pp. 52–60, jan. 2008.

[4] e. Men sink, d. Schinkel, e. A. M. Klumperink, e. Van tuijl, and b. Nauta, "power efficient gigabit communication over capacitively driven rc-limited on-chip interconnects," ieee j. Solid- state circuits, vol. 45, no. 2, pp. 447–457, Feb. 2010.

[5] d. Schinkel, e. Men sink, e. A. M. Klumperink, e. V. Tuijl, and b. Nauta, "low-power, high- speed transceivers for network-on-chip communication," ieee trans. Very large scale integer. (vlsi) syst., vol. 17, no. 1, pp. 12–21, jan. 2009.

[6] j. Park, j. Kang, s. Park, and m. P. Flynn, "a 9-gbit/s serial transceiver for on-chip global signaling over lossy transmission lines," ieee trans. Circuits syst. I, reg. Papers, vol. 56, no. 8, pp.1807–1817, Aug. 2009.

[7] m. P. Flynn and j. J. Kang, "global signaling over lossy transmission lines," in proc. Ieee/acmint. Conf. Compute.-aided design (iccad, Nov. 2005, pp. 985–992.

[8] h. G. Rhew, m. P. Flynn, and j. Park, "a 22 gb/s, 10 mm on-chip serial link over lossytransmission line with resistive termination," in proc. Esscirc (esscirc), 2012, pp. 233– 236.

[9] n. Tzartzanis and w. W. Walker, "differential current-mode sensing for efficient on- chip global signaling," ieee j. Solid-state circuits, vol. 40, no. 11, pp. 2141–2147, Nov. 2005.

[10] Maheshwari and w. Burleson, "differential current-sensing for on-chip interconnects," ieee trans. Very large scale integer. (vlsi) syst., vol. 12, no. 12, pp. 1321– 1329, Dec. 2004.

[11] C.Nagarajan and M.Madheswaran - 'Experimental verification and stability state space analysis of CLL-T Series Parallel Resonant Converter' - Journal of ELECTRICAL ENGINEERING, Vol.63 (6), pp.365-372, Dec.2012.

[12] C.Nagarajan and M.Madheswaran - 'Performance Analysis of LCL-T Resonant Converter with Fuzzy/PID Using State Space Analysis'- Springer, Electrical Engineering, Vol.93 (3), pp.167-178, September 2011.

[13] C.Nagarajan and M.Madheswaran - 'Stability Analysis of Series Parallel Resonant Converter with Fuzzy Logic Controller Using State Space Techniques'- Taylor & Francis, Electric Power Components and Systems, Vol.39 (8), pp.780-793, May 2011.

[14] C.Nagarajan and M.Madheswaran - 'Experimental Study and steady state stability analysis of CLL-T Series Parallel Resonant Converter with Fuzzy controller using State Space Analysis'- Iranian Journal of Electrical & Electronic Engineering, Vol.8 (3), pp.259-267, September 2012.

[15] Nagarajan C., Neelakrishnan G., Akila P., Fathima U., Sneha S. "Performance Analysis and Implementation of 89C51 Controller Based Solar Tracking System with Boost Converter" Journal of VLSI Design Tools & Technology. 2022; 12(2): 34–41p.

[16] C. Nagarajan, G.Neelakrishnan, R. Janani, S.Maithili, G. Ramya "Investigation on Fault Analysis for Power Transformers Using Adaptive Differential Relay" Asian Journal of Electrical Science, Vol.11 No.1, pp: 1-8, 2022.

[17] G.Neelakrishnan, K.Anandhakumar, A.Prathap, S.Prakash "Performance Estimation of cascaded h-bridge MLI for HEV using SVPWM" Suraj Punj Journal for Multidisciplinary Research, 2021, Volume 11, Issue 4, pp:750-756

[18] G.Neelakrishnan, S.N.Pruthika, P.T.Shalini, S.Soniya, "Perfromance Investigation of T-Source Inverter fed with Solar Cell" Suraj Punj Journal for Multidisciplinary Research, 2021, Volume 11, Issue 4, pp:744-749

[19] C.Nagarajan and M.Madheswaran, "Analysis and Simulation of LCL Series Resonant Full Bridge Converter Using PWM Technique with Load Independent Operation" has been presented in ICTES'08, a IEEE / IET International Conference organized by M.G.R.University, Chennai.Vol.no.1, pp.190-195, Dec.2007

[20] M Suganthi, N Ramesh, "Treatment of water using natural zeolite as membrane filter", Journal of Environmental Protection and Ecology, Volume 23, Issue 2, pp: 520-530,2022

[21] M Suganthi, N Ramesh, CT Sivakumar, K Vidhya, "Physiochemical Analysis of Ground Water used for Domestic needs in the Area of Perundurai in Erode District", International Research Journal of Multidisciplinary Technovation, pp: 630-635, 2019