VLSI-Area and Power Efficient Truncate Booth Multiplers Using Approximate Carry Based Error Compensation

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ABSTRACT - Approximate computing is a promising technique to elevate the performance of digital circuits at the cost of reduced accuracy in numerous error-resilient applications. Multipliers play a key role in many of these applications. In this brief, we propose a truncation based Booth multiplier with a compensation circuit generated by selective modifications in k-map to circumvent the carry appearing from the truncated part. By judicious mapping, hardware pruning and output error reduction is achieved simultaneously. In the quest of power and accuracy trade-off, Truncated and Approximate Carry based Booth Multipliers (TACBM) are proposed with a range of designs based on truncation factor.

Keywords: Approximate Multiplier, Booth Multiplier, Vedic Multiplier.

I. INTRODUCTION

FIR filters are one of two primary types of digital filters used in digital signal processing (DSP) applications, the other type being IIR.High performance FIR filters have applications in several video processing and digital communications systems. In some applications, the FIR filter circuit must be able to operate at high sample rates, while in other applications, the FIR filter circuit must be a low-power circuit operating at moderate sample rates.

A finite impulse response (FIR) filter is a type of a digital filter. Here the impulse response is finite because it settles to zero in a finite number of sample intervals. This is in contrast to infinite impulse response (IIR) filters. IIR filters have internal feedback and may continue to respond indefinitely. The impulse response of an Nth-order FIR filter lasts for N+ 1 sample, and then dies to zero. The finite-impulse response (FIR) filter is one of the fundamental processing elements in any digital signal processing (DSP) system. FIR filters are used in DSP applications that range from video and image processing to wireless communications.

In some applications, such as video processing, the FIR filter circuit must be able to operate at high frequencies. But in some other applications, such as cellular telephony, the FIR filter circuit must be a lowpower circuit, capable of operating at moderate frequencies. Parallel, or block, processing can be applied to digital FIR filters to either increase the effective throughput or reduce the power consumption of the original filter. Traditionally, the application of parallel processing of an FIR filter involves the replication of the hardware units that exist in the original filter. If the area required by the original circuit is A, then the Lparallel circuit requires an area of L x A. With the continuing trend to reduce chip size and integrate multi-chip solutions into a single chip solution, it is important to limit the silicon area required to implement a parallel FIR digital filter in it VLSI implementation. In many design situations, the hardware overhead incurred by parallel processing cannot be tolerated due to limitations in design area. Therefore, it is advantageous to have parallel FIR filtering structures that consume less area than traditional parallel FIR filtering structures.

In this project we provide new reconfigurable FIR filter structures based on RFIR consisting of advantageous low power and low area , which can reduce amount of flip flops in the sub filter section by exploiting the inherent nature of the symmetric coefficients, compared to the existing FIR filter structure.

Digital Signal Processing. Digital signal processing (DSP) is the use of digital processing, such as by computers, to perform a wide variety of signal processing operations. The signals processed in this manner are a sequence of numbers that represent samples of a continuous variable in a domain such as time, space, or frequency. Digital signal processing and analog signal processing are subfields of signal processing. DSP applications has audio and speech signal processing, sonar, radar and other sensor array processing, spectral estimation, statistical signal processing, digital image processing, control of systems, biomedical engineering, seismic data processing, among others. DSP can involve linear or nonlinear operations. Nonlinear signal processing is closely related to nonlinear system identification and can be implemented in the time, frequency, and spatio-temporal domains. The application of digital computation to signal processing allows for many advantages over analog processing in many applications, such as error detection and correction in transmission as well as data compression. DSP is applicable to both streaming data and static data.

This project report is organized as follows. Section 2 investigates the literature survey. In Section 3, approximate multiplier structures are presented. Section 4 presents the design proposed reconfigurable approximate multiplier. Proposed structures are defined. Techniques are shown in Section 5 discusses system requirements. In

Chapter 6 simulation results are shown. The comparison of area and power are shown. Finally, the conclusion and future work is given.

II. LITERATURE SURVEY

Siyuan Xu , Many applications show tolerance to inaccuracies. These can be exploited to build faster circuits with smaller area and lower power. This is particularly true for the hardware accelerators in heterogeneous computing systems. A major problem with approximate computing is that the resulting approximated circuit is highly dependent on the training data. Previous works often rely on static training results. If the workload is dynamic in nature or changes over time, output errors may reach unacceptable levels. Therefore, dynamic control methods are needed to solve this problem. To address this issue, in this paper, we propose an approximate self-adaptive architecture that autotunes itself at runtime based on the workload.

Lucas Machado, Decomposition is a technology-independent process, in which a large complex function is broken into smaller, less complex functions. The costs of two-level or factored-form representations (cubes and literals) are used in most decomposition methods, as they have a high correlation with the area of cell-based designs. However, this correlation is weaker for field-programmable gate arrays (FPGAs) based on look-up tables. Furthermore, local optimizations have limited power due to the structural bias of the circuit descriptions. This paper tries to reduce the structural biasing by remapping the look-up table network and decomposing the derived functions using the support as cost function. Xiaoming Chen, As an emerging nonvolatile device, ferroelectric field-effect transistors (FeFETs) have the potential to reduce the power and area by integrating nonvolatile storage elements with logic. The hysteretic behavior allows an FeFET to function as both a nonvolatile storage element and a switch. This paper exploits this feature of FeFETs to design lookup tables (LUTs) and routing switches, which have obvious utility in field-programmable gate arrays (FPGAs).

M. Kang, Computing systems at all scales (from mobile handheld devices to supercomputers, servers, and large cloud-based data-centers) have seen significant performance gains, mostly through the continuous shrinking of the complementary metal–oxidesemiconductor (CMOS) feature size that has doubled the number of transistors on a chip with every technology generation. Gaurav Verma, Most of the computational tasks inside the processing element are performed by ALU circuit. ALU is considered as the computational engine and responsible for high power consumption. Previously, microprocessors and microcontrollers were the choice of designers but nowadays the horizon has been shifted to FPGAs and SOCs as a processing element in mobile devices.

Reconfigurable technology fits for real-time video streaming applications. It is considered as a promising solution due to the offered performance per watt compared to other technologies. Since FPGA evolved, several techniques at different design levels starting from the circuit-level up to the system-level were proposed to reduce the power consumption of the FPGA devices. In this paper, we present a flexible parallel hardware-based architecture in conjunction with frequency scaling as a technique for reducing power consumption in video streaming applications. In this work, we derived equations to ease the calculation for the level of parallelism and the maximum depth for the FIFOs used for clock domain crossing. Accordingly, a design space was formed including all the design alternatives for the application. The preferable design alternative is selected in aware of how much hardware it costs and what power reduction goal it can satisfy. This fundamental trade-off benefits particularly well from the tile-based structures of modern FPGAs that consist of large number of redundant logic cells. Using the design of a comparator as an example, we study the trade-offs and unique opportunities provided by modern FPGA architectures in employing precomputation as a technique to reduce dynamic power consumption.

After realizing the inefficiency of traditional buses in SoCs, in conjunction with so many other factors, the designers of SoCs have come to a cross-road where they meet the computer architecture designers who are always interested in finding dynamic and scalable architectures for building microprocessors. The scalability and wide success of the Internet has attracted the attention of computer architecture as well as SoC designers and influenced them to borrow the idea of using packet based switching networks for the design of future SoC communication infrastructure. It is an understood fact that the actual reason behind success of the Internet and its scalability lies in a well-defined protocol stack; the idea was to decouple communication from computation.

III. PROPOSED SYSTEM

The advent of approximate computing has opened new avenues for enhancing the efficiency of digital circuits, particularly in error-resilient applications where a compromise between computational accuracy and performance is acceptable. Multipliers are essential components in various such applications, motivating the exploration of innovative approaches to improve their efficiency. In this context, the proposed Truncated and Approximate Carry-based Booth Multipliers (TACBM) introduce a truncation-based methodology with a compensation circuit designed through selective modifications in the k-map. This compensates for the carry introduced by the truncated portion of the multiplier, achieving simultaneous hardware pruning and output error reduction.

Digital circuits are integral components in modern computing systems, and enhancing their performance is a continuous pursuit. The abstract introduces the concept of approximate computing as a technique to boost the

efficiency of digital circuits, albeit at the expense of reduced accuracy in error-resilient applications. Within this context, the focus is on multipliers, which play a pivotal role in numerous applications. This proposed system aims to introduce a novel Truncated and Approximate Carry-based Booth Multiplier (TACBM) as a solution to strike a balance between power consumption and computational accuracy.

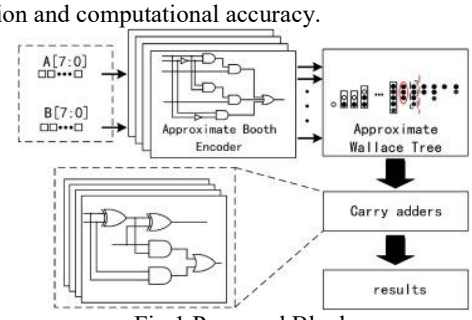

Fig.1 Proposed Block

The proposed system begins by addressing a specific challenge associated with approximate computing—the introduction of a truncation-based Booth multiplier with a compensation circuit generated through selective modifications in the Karnaugh map (k-map). The truncation process is fundamental in approximate computing, and the compensation circuit is designed to circumvent the carry introduced from the truncated part. This unique approach contributes to achieving simultaneous hardware pruning and output error reduction. The system leverages judicious mapping techniques, allowing for efficient handling of errors while maintaining computational efficiency. Comparative analysis with state-of-the-art multipliers forms a crucial aspect of the proposed system's validation. TACBM emerges as a frontrunner, showcasing superior performance in terms of both accuracy and Area-Power savings. The evaluation of TACBM at =10 reveals compelling results, with a mere 0.02% Mean Relative Error of Difference (MRED) and a substantial 23% reduction in the Area-Power product compared to an exact Booth multiplier. This evidence underscores the effectiveness of the proposed system in achieving a favorable balance between accuracy and power efficiency.

IV. RESULTS

In this section, the hardware overheads and accuracy of the proposed approximate 16-bit multiplier designs are assessed. Meanwhile, the performance of the accurate and several other approximate Booth multipliers are compared with the proposed designs.The multipliers are structurally modelled in Verilog HDL. The simulation and synthesis are done in Xilinx® ISE 14.7. A comparison on the basis of area, power and delay is performed on Virtex-6 (XC6VLX75TL FF784 -1). The entire structure is same for the floating point multiplier designs except for the 24x24 multiplier block, which will be designed with separate integer multipliers. Hence area and speed of the floating point multipliers depends on the performance of the integer multipliers.The Vedic Multipliers consume more area than proposed booth multipliers. It is expected due to the presence of three adder structures and four 16x16 multipliers, each of which in turn contains 8x8 multiplier structures and so on.

The Booth Multipliers are found to be having more speed than other multipliers. This is due to the partial products are generated and summed in parallel. Also the delay associated with the Multipliers is mainly due to the propagation of carry bits through adders. Booth multiplication is smaller, faster multiplication algorithm through encoding the signed numbers, which is also a standard technique used in chip design, and provides significant improvements by reducing the number of partial product to half over “long multiplication” techniques. After performing the synthesize process, the RTL schematic has been created automatically based on the functionality. The routing between the different cells can be viewed clearly by this schematic.

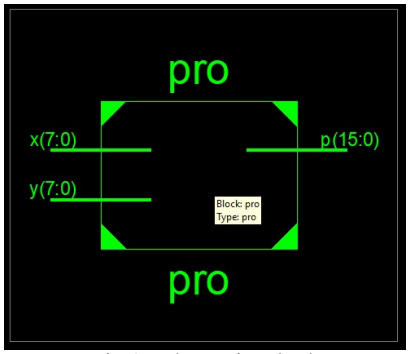

Fig.2 Schematic Block

Fig.3 RTL Schematic Block

In this module, the power, area and delay analysis are obtained, and the results are compared. The power, area and delay analysis have been made using Xilinx ISE 14.7. The results for are shown in the table 1:

Table. 1 Comparative Analysis of Power, Area & Delay on Proposed

Module	Power Consumption (mW)	Area (Device Utilization)			Delay (nS)
		IOB	LUT	FF	
Existing Vedic	0.801	32	140	120	7.758
Proposed Booth Multiplier	0.065	32	96	96	7.137

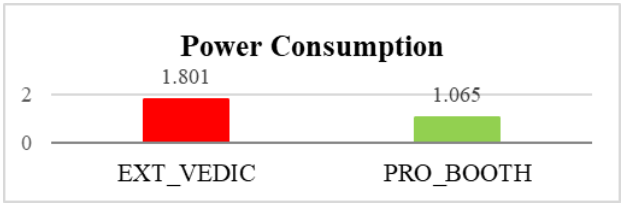

Fig.4 Power Analyses

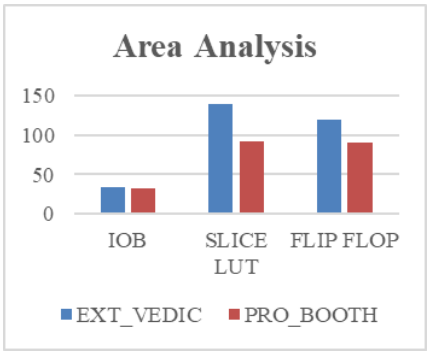

Fig.5 Area Analysis

V. CONCLUSION

In conclusion, the proposed Truncated and Approximate Carry-based Booth Multipliers (TACBM) represent a significant advancement in the realm of approximate computing, offering a compelling solution to the power and accuracy trade-off in digital circuits. The utilization of a truncation-based Booth multiplier, coupled with a compensation circuit derived through selective modifications in the Karnaugh map, demonstrates a judicious approach to mitigate the impact of carry introduced from the truncated part. The concurrent achievement of hardware pruning and output error reduction highlights the efficiency of the proposed system.

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