Design of Low Power and Area Efficient Carry Select Adder using 8T Full Adder

S. Kalaiabinaya, S.Shalini, G.Suji, E.Vaishnavi, R.Prabu
Associate Professor of ECE
Paavai College of Engineering

Abstract-The Fastest adder among regular adder structure is known as Carry select adder (CSLA) in many data-processing processors to perform fast arithmetic functions. In this modified square root CSLA involves Binary Adder and 3T-XOR gate based 8T full adder design to reduce the number of transistors in the adder circuit. This work uses a simple and efficient Gate-Level modification to significantly reduce the area and power of the CSLA. The proposed design has reduced area and power as compared to regular CSLA and modified CSLA. An area of proposed 8-bit CSLA is reduced by 27.1% and 5.45% when compared with R-CSLA and M-CSLA, respectively. The proposed architecture achieves the advantages in terms of delay, area and power. In this project Xilinx-ISE tool is used for simulation and Micro wind Tools for Power analysis.

I. INTRODUCTION

Now a days VLSI circuit designs, there is a significant increasein the power consumption due to the complexity andincreasing speed of the circuits. Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. An adder with low power and fast addition operation along with low area consumption is still a challenging problem. Depending upon the area, delay, and power consumption, the various adders are categorized as ripple carry adder (RCA), carry select adder (CSLA), and carry look ahead adder (CLAA). CSLA provides a compromise between the large area with small delay of CLAA and small area and longer delay of RCA [8].

CSLA uses pair of RCAs for addition, that is, one block of RCA with Cin (carry in) = 0 and other block of RCA with C_{an} = 1. Depending on the value of previous carry, the final sum and carry outputs are selected using multiplexer. Due to the pair of RCAs used for each bit addition, the simplest kind of CSLA is not very efficient [9].The basic idea of this work is to use Binary adder instead of BEC and RCA with C_{an}=1 in the M-CSLA and regular CSLA to achieve lower area and power consumption [2]–
[4]. The main advantage of this Binary adder logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. The details of the Binary adder logic are discussed in Section V. The XOR gates are the building blocks of adders, here in this work; we use a 3T-XOR gate and Binary adder to design an 8-bit CSLA. The main advantage of using 3T-XOR gate is that the power consumption of the circuit decreases due to the large decrease in number of switching transistors (MOSFETs) used in the design of 8-bit CSLA.

II. DELAY AND AREA CALCULATION OF THE BASIC ADDER BLOCKS.

The Inverter, AND & OR based implementation of an XOR gate is shown in Figure.1. The gates between the dotted lines are performing parallel operation and the representation of each gate indicates the delay by that gate. The delay and area calculation considers all gates to be made up of AND, OR, and Inverter, each gate having delay equal to 1 unit and area equal to 1 unit.

The area evaluation is completed by counting the total number of AOI gates required for each logic block. Based on this Concept, the CSLA adder blocks of 2:1 mux, Half Adder (HA), FA and BEC are evaluated and listed in Table I.

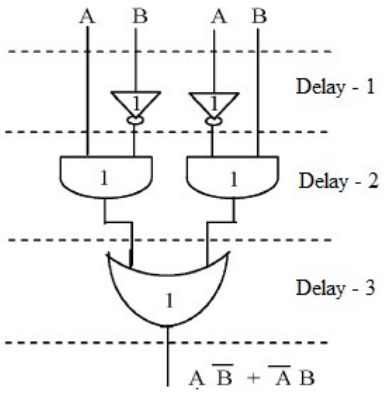


Figure.1: Delay and Area calculation of an XOR gate.

Table I: Delay and Area of Logic gate Count of The Basic Blocks.

Adder Blocks	Delay	Area
XOR	3	5
MUX 2:1	3	4
Half adder	3	6
Full adder	6	13
BEC -3 bit	4	12
BEC -4 bit	5	18

III. EARLIER WORKS ON CARRY SELECT ADDER

A. Delay and Area Calculation of Regular 8-Bit SQRT CSLA

The structure of the 8-bit regular SQRT CSLA is shown in Figure.2. It has four stages of different size RCA. The delay and area calculation of each group are shown in Figure.2, in which the numerals delay values are specify in Table II.

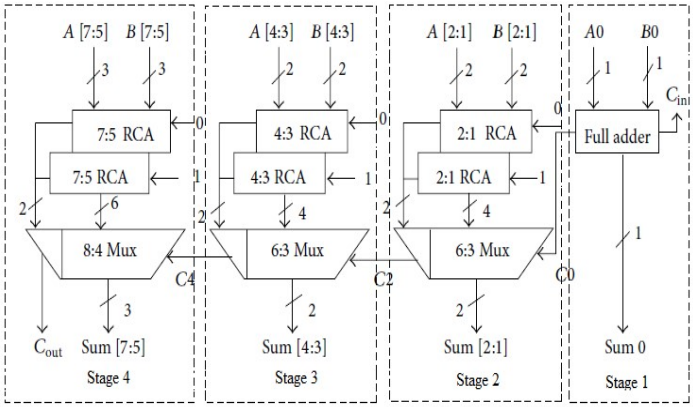


Figure.2: Regular 8-bit CSLA.

In adders, the speed of addition is limited due to the time taken by the carry propagate through the adder. The regular carry select adder (R-CSLA) was introduced to mitigate the problem of carry propagation delay by independently generating multiple carries and then selecting the correct sum and carry outputs depending on the value of previous carry [9]. As previously discussed, this type of CSLA (i.e., R-CSLA) was not area efficient due to the use of pair of RCAs (each for Cin = 0 and Cin = 1) to produce the final sum and carry output. The 8-bit R-CSLA is shown in Figure 2.

Table II: Delay and Area of Logic gate Count of Regular 8 bit CSLA Stages.

Stages	Delay	Area	
		FA	MUX
Stage 1	6	13	0
Stage 2	11	45	12
Stage 3	13	45	12
Stage 4	16	71	16
Total		174	40
		Area = 214	

B. Delay and area evaluation methodology of modified 8-bit SQRT CSLA

The structure of the modified 8-bit SQRT CSLA using BEC for RCA with $C_{an} = 1$ to optimize the area and power is shown in Figure.4. We again split the structure into four stages. The delay and area calculation of each stages are shown in Figure.4.

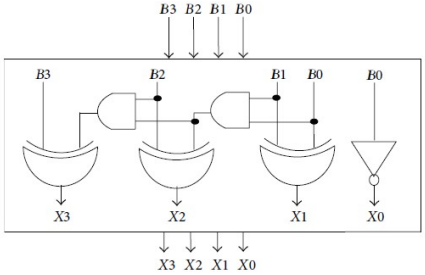


Figure 3: Four-bit BEC circuit

To make low power consumption and an area efficient CSLA, an add-one circuit known as Binary to Excess-1 Converter (BEC) circuit was introduced. This BEC circuit replaced the RCA with Cin = 1 used in R-CSLA as lesser numbers of logic gates were used in BEC as compared to n- bit RCA [10–12]. The circuit diagram of 4-bit BEC is shown in Figure 3. The 8-bit modified carry select adder (M-CSLA) using BEC is shown in Figure 4.

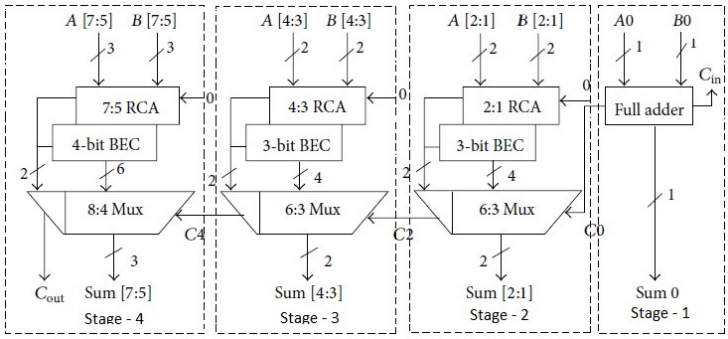


Figure 4: Modified 8-bit CSLA with BEC.

An 8-bit M-CSLA was divided into four stages with different bit sizes of RCA and BEC. M-CSLA consists of RCAs (for Cin = 0), BEC circuits (for Cin = 1), and multiplexers (MUX). One input to the MUX is sum along with carry outputs from RCA and another input to the MUX is sum along with carry outputs from BEC circuit. The final sum and carry outputs are selected depending upon the value of previous carry which is inputted as the select line to the MUX [10].

Table III: Delay and Area of Logic gate Count of Modified CSLA with BEC Stages

Stages	Delay	Area		
		FA	MUX	BEC
Stage 1	6	13	0	0
Stage 2	13	19	12	12
Stage 3	16	19	12	12
Stage 4	19	32	16	18
Total		83	40	42
		Area = 165		

IV. MODIFIED WORK ON CARRY SELECT ADDER

This work is realization of low power operation of the conventional CSLA circuit through logic binary adder operation. The modified work replaces the second *n-bit RCA with (Can=1)* of the SQRT CSLA architecture shown in Figure.5, with an n-bit binary adder used as *BEC-1*. The modified further employs OR gates, which is only the minimum overhead required in place of the multiplexers used in SQRT CSLA and CSLA using BEC-1. The OR structure along with *n*-bit binary adder results in generating BEC-1 operation, even while employing reduced device count and simpler architecture.

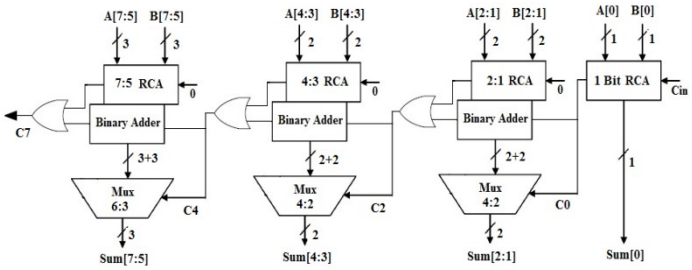


Figure 5: Modified 8-bit CSLA with Binary Adder.

Table IV: Delay and Area of Logic gate Count of Binary adder based CSLA Stages.

Stages	Delay (Carry)	Area		
		FA	MUX	BA & OR
Stage 1	6	13	0	0
Stage 2	8	19	8	13
Stage 3	11	19	8	13
Stage 4	15	32	12	19
Total		83	28	45
		Area = 156		

The modified 8-bit CSLA has been successfully tested and synthesized in Xilinx Tool. The power consumption and delay time of proposed 8-bit CSLA is calculated using Logic gate Count of The Basic Blocks. The power consumption and delay time of modified 8-bit CSLA are compared with 8-bit R-CSLA and M-CSLA. The comparison is shown in Table [I - IV]. It is clear from Table IV that area of modified 8-bit CSLA is reduced by 27.1% and 5.45% when compared with R-CSLA and M-CSLA, respectively.

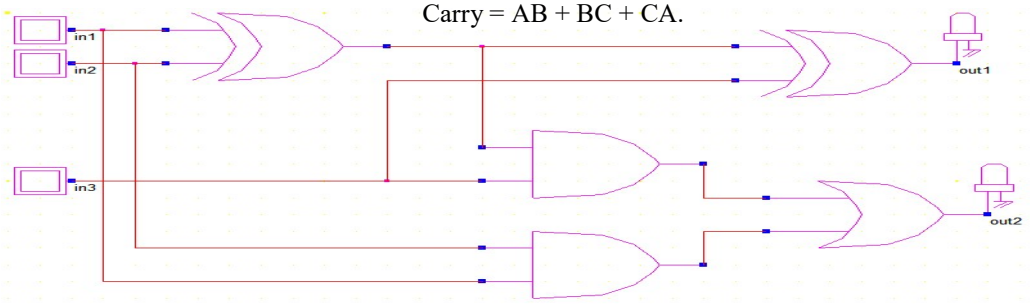
V. PROPOSED WORK ON CSLA

A. Conventional Full Adder and NAND based Full adder:

A full adder is under comes in the category of combinational circuits which adds upto three binary digits. The design of full adders which forms the basic building blocks of all digital VLSI circuits.Conventional Equations of outputs of a full adder are:

Sum = A x or B x or C

Carry = AB + BC + CA.



Adder

Figure.6: Logic diagram of Full

B. Three-Transistor XOR Gate:

XOR gate is the basic building block for full adder. 3T XOR Gate used in this design shown in figure. The XOR consists of three transistors which are two PMOS and one NMOS. Design is based on a modified version of a CMOS inverter and a PMOS pass transistor. When the input B is at logic high, the inverter on the left functions like a normal CMOS inverter. Therefore the output Y is the complement of input A.

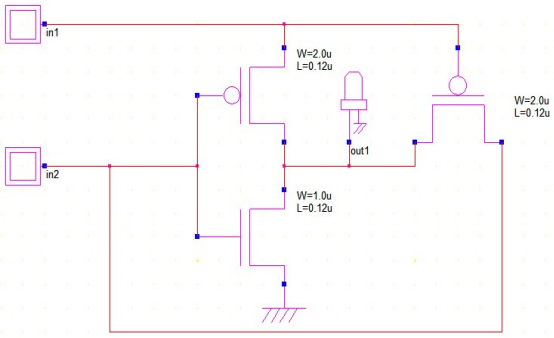


Figure.7: Logic diagram of 3T XOR gate

When the input B is at logic low, the CMOS inverter output is at high impedance. However, the pass transistor M3 is enabled and pass the output Y gets the same logic value as input A. The operation of the whole circuit is thus like a 2 input XOR gate.

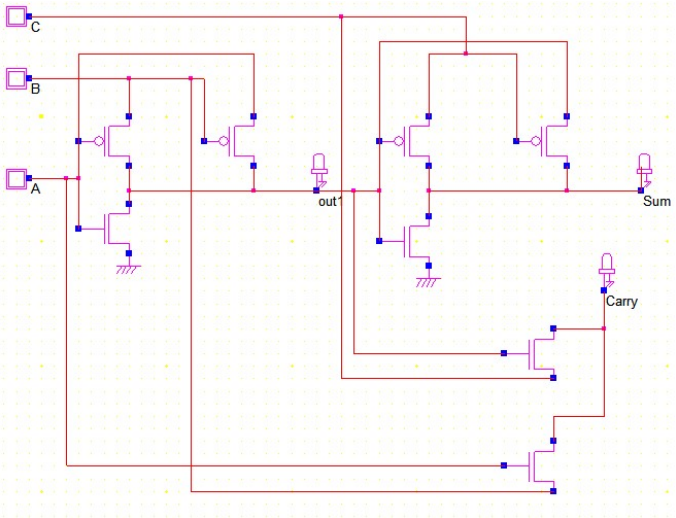


Figure.8: Logic Diagram of Full adder using 3T XOR gate based 8T FA.

C. Binary Adder

The main idea of this work is to use BA instead of the RCA with C_{an} = 1 and BEC in order to reduce the area and power consumption of the regular CSLA. To replace the n - bit RCA and n + 1 bit BEC, a Binary adder is required. A structure of 4-bit BA are shown in Figure.10.

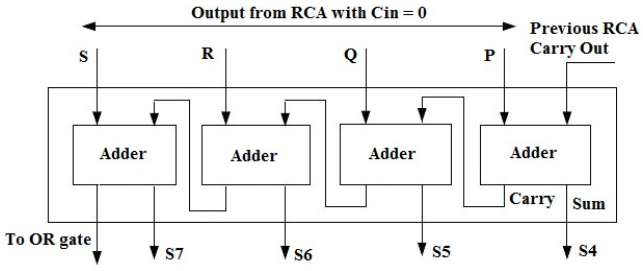


Figure.9: 4 bit Binary Adder

D. Proposed 8-bit CSLA with binary adder using 3T XOR gate based 8T

In thiswork, we useamodifiedXOR gate as it forms the basic building block of CSLA.Here, we use a 3-TXOR gate instead of BEC and RCA gate used in previous designs of R-CSLA and M-CSLA which helps in more efficient design of 8-bit CSLA [13].The circuit diagram of 3-T XOR gate and proposed 8-bit CSLA are shown in Figures 10 and 11, respectively.

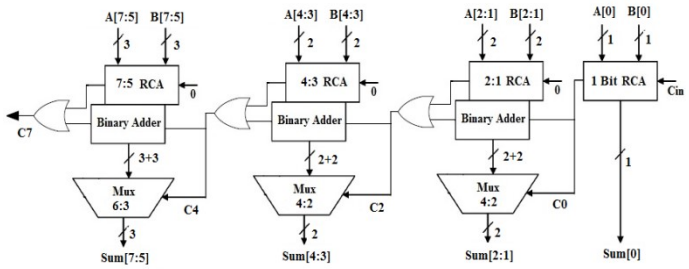


Figure.10: Architecture of 8-bit CSLA with binary adder using 3T XOR gate

The overall performance of CSLA in terms of power consumption, transistor count, and power-delay product (PDP) can be enhanced by modifying the XOR gate. A single modified XOR gate (3-T XOR gate) used in this work has 9 lesser transistors as compared to the XOR gate (12-T XOR gate) used in earlier works on CSLA. The proposed 16-bit CSLA is divided into 4 stages as shown in Figure 11.

The total reduction in transistor and Mux count for each stage is calculated below.

Stage 1. It contains one full adder. Each full adder consists of two XOR gates. Therefore total transistor count reduction for stage 1 is
Number of XOR gates used = 2;
Total No.of Transistor are reduced in this stage = 18 $(2 * 9)$.

Stage 2. It contains one full adder, one half adder, and Two half adder. The transistor count reduction for stage 2 is as follows:
Number of XOR gates used = 5 (2 + 1 + 2);
Total No.of Transistor are reduced in this stage = 45 $(5 * 9)$.
Total No.of Mux reduced = 1

Stage 3. It contains one full adder, one half adder, and Two half adder. The transistor count reduction for stage 2 is as follows:
Number of XOR gates used = 5 (2 + 1 + 2);
Total No.of Transistor are reduced in this stage = 45 $(5 * 9)$.
Total No.of Mux reduced = 1

Stage 4. It contains two full adders, one half adder, and one 4-bit BEC. The transistor count reduction for group 4 is as follows:
Number of XOR gates used = 8 $\{(2 * 2) + 1 + 3\}$;
Total No.of Transistor are reduced in this stage = 72 $(8 * 9)$.
Total No.of Mux reduced = 1

Therefore the overall reduction in number of switching transistors (MOSFETs) in proposed 8-bit CSLA as compared to the previously designed 8-bit M-CSLA is 3 Mux and 180 Transistor. Hence, the reduction in number of switching transistors reduces the power dissipation of 8-bit CSLA.

VI. SIMULATION RESULT

6.1 Simulation Output

In this study, Simulation of 32 bit 8T Based Carry Select Adder with Binary Adder is implemented in Verilog HDL and logic simulation is done by using Model Sim Software.

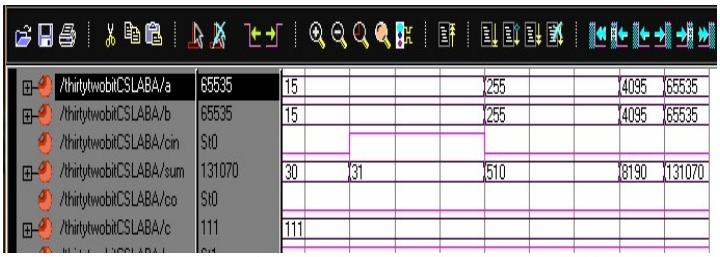


Figure.6.1: Simulation results for 32-bit 8T based Carry Select Adder with BA.

Simulation of 8 – bit Carry Select Adder with Binary Adder is implemented in Verilog HDL and simulation is done by using Xilinx ISE 13.2.

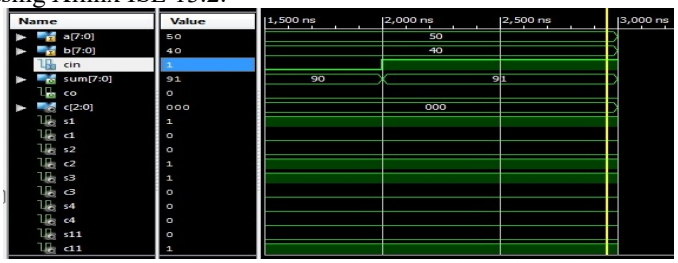


Figure.6.2: Simulation results for 8-bit Carry Select Adder with BA.

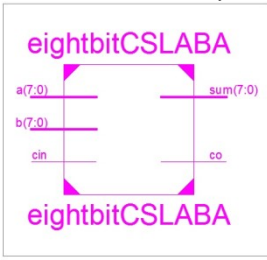


Fig.6.3: RTL Simulation Block Diagram of 8-bit Carry Select Adder with BA.

6.2. Comparative Analysis

Various types of Adders in terms of Delay, Area and No. of LUT Flip Flop pairs. It is shown in Table IX.

Table 6.1: Observations of Various Adders:

Parameter	Ripple Carry Adder (RCA)	Carry Select Adder (CSLA)	Carry Select Adder (BEC)	Carry Select Adder (BA)
Delay (8 bit)	2.523ns	2.787ns	2.046ns	2.841ns
No. of LUT-Flip Flop pairs (8 bit)	12	12	16	15
Area (16 bit)	910	1620	1268	762
Memory (Kilobytes)	223980	223980	218028	218476

6.3. SIMULATION OF DSCH & MICROWIND TOOL

The schematic circuit of the Full Adder have been designed using DSCH Simulator Tool and Synthesized using 0.12µm CMOS Technology. The layout was constructed from the Verilog file which is generated from the DSCH Software. The obtained power, area and delay information of the adder is from Micro wind layout simulation.

Table 6.2: Shows the Simulation results of both conventional and modified FA (using 3T XOR based 8T full adder) in terms of power.

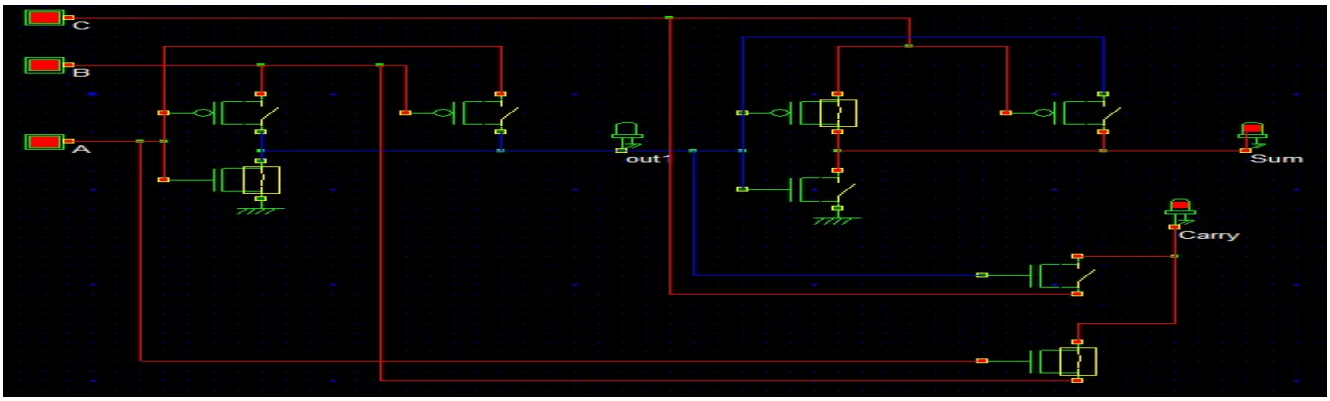


Figure.6.4: Digital Schematic (DSCH) of 3T XOR based 8T Full Adder.

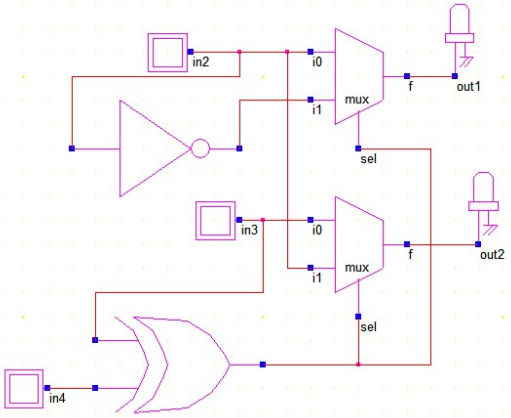


Figure.6.5: Digital Schematic (DSCH) of MUX based Full Adder

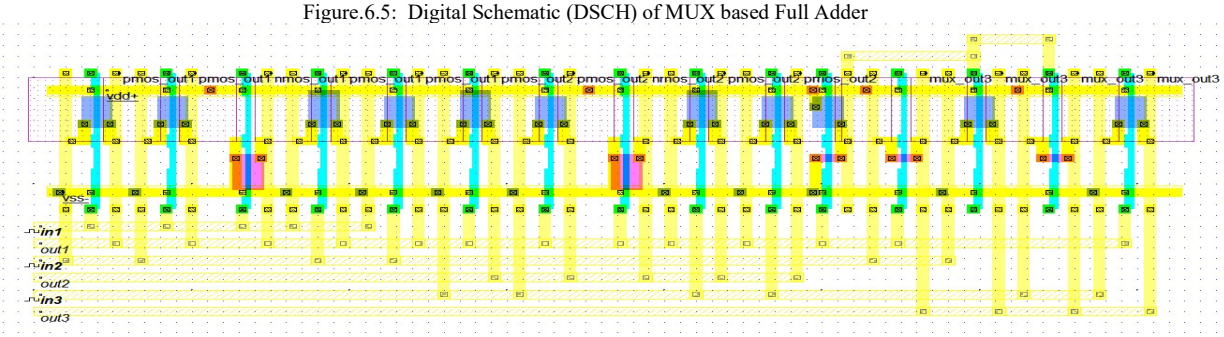


Figure.6.6: Layout of 3T XOR based 8T Full Adder

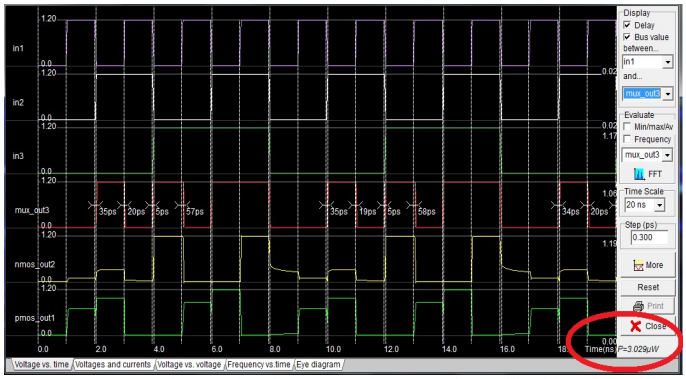


Figure.6.7: Simulation of Voltages Vs Time (One bit Full Adder using 8T)

6.5. Comparison Chart of MUX and 8T based Full Adders for Power:

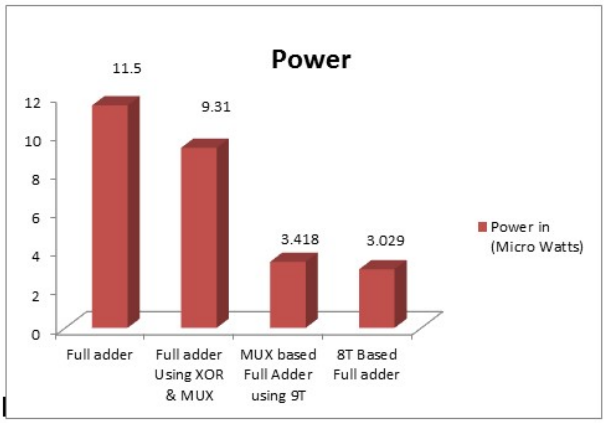


Figure.6.8: Power Analysis

Table 6.2: Simulation Result of Various Full adder:

Parameter	Full Adder	Full Adder using XOR & MUX	MUX based Full Adder using 9T	Full Adder using 8T
Power	11.5µw	9.31µw	3.418 µw	3.029µw

VII. CONCLUSION

A simple methodology of improving the performance of Binary Adder and 3T XOR gate based 8T full adder to design an 8-bit CSLA is used in this paper. The proposed CSLA has large decrease in switching transistor due to the use of 8-T full adder. On comparing this proposed 8-bit CSLA with other existing 8-bit CSLAs like R-CSLA and M-CSLA, there is 27.5% and 5.45% reduction in Area, respectively. Also reduced number of gates of this work offers the great advantage in the reduction of total power. The modified CSLA architecture is therefore, low area, low power, simple and efficient for VLSI hardware implementation.

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