Genetic Algorithm based Thermal Aware Don't Care Filling to Reduce Peak Temperature and Thermal Variance during Testing

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Abstract: Due to the rapid increase in VLSI technology, device contains hundreds of million transistors. Shrinking of feature size and increased device density leads to more power consumption during testing. The power dissipation during testing is higher than normal mode of operation which increases the temperature. Increase in temperature and power dissipation causes permanent damage of a chip. Power dissipation can be reduced by reducing the switching activity of the circuit under test which leads to less temperature during testing. Reducing the switching activity of the whole circuit does not help to reduce the localized heating which is called as "Hotspot". Temperature of the block depends on both temperature of that block and temperature of the neighbouring blocks. So reduction in peak temperature has become necessary to bring the uniformity in heat dissipation. To reduce peak temperature don't care bits which are present in the test pattern set are filled to reduce switching activity of the block and also its neighbouring blocks. Various X-filling techniques has been proposed like 0-filling, 1-filling and MT-filling. In this paper thermal aware Genetic Algorithm based X-filling algorithm is proposed to reduce peak temperature and peak power. S27 and S953 Benchmark circuits are simulated using the two algorithm and the experimental results are compared with other X-filling techniques.

Keywords: Hotspot, Criticality, Don't care filling, Genetic Algorithm, ATPG

I. INTRODUCTION

Integrated Circuits have grown in size and complexity since the late 1950's. Moore's Law states that the number of transistors in IC has doubled every 18 months. Decrease in feature size increases the probability of defects during manufacturing process. With the expeditious progression in IC technology a VLSI device now contains thousands and thousands of transistors in a single IC. Such growth increases the complexity of the VLSI circuits and testing. Because of Shrinking in feature size and increase in device complexity the power consumption during testing has become very important. The power dissipation during testing is much higher than during normal mode of operation [14]. Higher test power may lead to permanent or temporal damage of the chip.

Test power is quantified by two metrics such as Average power and Peak Power. Average test power is the ratio between the total energy dissipated during testing and the total test time. Peak power is defined as the maximum instantaneous power in any given clock cycle during testing. High average test power may cause permanent damage to chip and package due to the high heat dissipation. On the other hand, high peak power causes voltage drop and power/ ground noise that results in circuits malfunctioning only during testing and hence yield loss. Higher power consumption leads to higher heat dissipation. Majority of the power reduction techniques are oriented towards reducing the dynamic power consumption. Excessive switching activity increases the overall circuit temperature and also creates localized heating, called hotspots [5]. Minimizing power consumption can reduce overall temperature of the CUT. However this may not minimize the peak temperature due to non-uniformity in the power distribution. Minimizing the overall switching activity does not help to reduce the peak temperature on hotspots. Peak Temperature of a block depends on both heat dissipation of the block and heat dissipation of neighbouring blocks in the circuit under test (CUT). So temperature difference arises across the circuit. To bring uniformity in the temperature distribution across

the chip, the power consumption across the chip should be uniformly distributed so that thermal variance across the chip can be minimized.

Various methods have been discussed in literature to reduce to power [1][2][7][10][11][15]. Don't care bits in the test pattern set are filled in order to reduce the peak temperature. With increasing chip density, power aware X-filling is proved inadequate and has to be replaced by thermal aware X-filling techniques.

In this paper we have proposed Genetic algorithm based don't care filling to reduce the peak temperature as well as to bring uniformity in distribution of temperature. Genetic algorithm based don't care filling algorithm is applied to the ISCAS89 benchmark circuits and the results are compared.

The rest of the paper is framed as follows. In Section II, we have discussed about the steps for thermal simulation. In Section III Fitness function used to evaluate the patterns. In section IV the thermal aware don't care filling algorithm has been presented. In section V Genetic algorithm based don't care filling algorithm is discussed. In section VI experimental results are discussed. In Section VII conclusion and future work of the paper is presented

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II. Steps For Thermal Simulation

The temperature of an Integrated Circuit(IC) can be estimated by thermal simulation. The steps for the thermal simulation of a circuit with a set of test patterns are given in the following section.

- Circuit in Verilog format is taken as a input. The design is compiled using the Design Vision [3] logic synthesis tool from Synopsys. The gate level Netlist is the output from the compilation of original verilog format.
- The resulting netlist is now subjected to the scan mode compilation of the Design Vision tool to insert scan chain into the design for testability purpose. After design rule check and scan chain insertion, the netlist so obtained can be used for floorplan generation purposes
- To create the floorplan the netlist with scan cells obtained from Design Vision is given to the IC compiler of Synopsys Tool [6].
- Test set with don't care bits for the design is generated using any Automated Test Pattern Generation (ATPG). Tetramax[13] ATPG tool is used for this purpose.
- The scan inserted netlist and the test pattern set is now used to estimate the power of the each blocks. The scan inserted netlist is simulated using ModelSim and output of each block is noted. From the outputs the total switching activity of each block is calculated. Power of each gate present in the design is estimated using Design Vision tool. The total switching activity is multiplied by the dynamic power of the gate to estimate a total dynamic power. Number of times the gate not switched also calculated and multiplied by the leakage power of that gate to estimate total leakage power. Total power of the block is estimated by adding the total dynamic power and total leakage power.
- The floorplan obtained from the IC_compiler and the power estimated for each block in the floorplan is now given to the HotSpot tool [12]. Floorplan consists of Width and height of each block. The temperature of each block is calculated from the Floorplan and power trace file.

III. Fitness Calculation

A. Estimation of Thermal Behaviour

The power estimation does not take care of floorplan information, which is necessary for temperature aware solutions. The term, criticality is used to find the temperature estimation. Criticality for a block is actually a measure of "how hot" that block can be during testing. Criticality (CRbi), for a particular block bi, is calculated by including bi and taking the average of power (P) values of the neighbouring blocks of bi. Criticality of block bi is now defined as

$$CR_{bi} = (P_{bi} + P_{ne(bi)})/(N+1) \quad (1)$$

Where,

N is the Number of Neighbouring blocks

P_{bi} is the power of the block bi

$P_{ne(bi)}$ is the total power of the neighbouring blocks of the block bi

Equation (1) is used to calculate the Criticality (CRbi) of a block bi which is used as the temperature estimator for the block bi.

B. Fitness Function

The aim of the problem is to reduce the peak temperature for the circuit during testing. So the block with maximum estimated temperature is found out and try to minimize it. Thus, the fitness function of the given problem is defined as:

$$\text{Fitness (C)} = \text{MAX (CRbi)} \qquad (2)$$

Equation (2) is used to calculate the fitness function. Don't care bits in the test set is filled based on the algorithm. The fitness is calculated for each pattern. Test pattern with minimum fitness value is selected.

IV. THERMAL AWARE DON'T CARE FILLING ALGORITHM

A.Algorithm to Fill Don't Care Bits

An algorithm [4] to fill the X-bits in the test pattern set is shown below. Input to this algorithm is test set with unspecified values. Output of this algorithm is test set with fully specified test set with minimum peak temperature.

1. Different filling techniques are applied to initial set with don't care bits and the test set with Minimum temperature is taken as a initial test set
2. Find C
3. Set org_c=C
4. for all t_j in test set TS do
5. for every X bits in t_j
6. Flip the bit from its originally filled value
7. Calculate C with modified test pattern and store it in temp_c
8. if temp_c < org_c
9. retain the flip
10. set org_c=temp_c
11. else
12. flip the bit back to original filled value
13. end for
14. end for
15. Output with fully specified patterns

Initially the test patterns with don't care bits are generated using ATPG tool. For a unspecified pattern set, 0 filling, 1-filling and minimum transition (MT) filing techniques are applied to produce three different test set from the initial incompletely specified test set. Thermal simulations have been carried out for each of the test set. The test set which has produced the minimum peak temperature has been found out. This test set is used as the initial test set for the algorithm. The reason to choose this approach is because the corresponding filling will lead to minimum peak temperature for that particular circuit. The selected pattern set is used to find out the fitness function. The calculated fitness value is assigned to org_c.

Next, a pattern from the pattern set is selected and the filled don't care bits is flipped one at a time to its complemented value. Now, the Fitness value is calculated with the new set. The computed fitness function value is assigned temp_c. If temp_c is lower than org_c, the particular flip is retained and temp_c value is assigned to org_c. Otherwise, the flipped bit is switched back to the original filled value. The procedure is repeated for every test pattern. Temperature of every block is calculated with the finally obtained test pattern set. With the obtained temperature the peak temperature of the CUT is calculated.

V. GENETIC ALGORITHM BASED DON'T CARE FILLING

Genetic Algorithm [9] is an evolutionary algorithm based on the evolutionary ideas of natural selection and genetics. It is a random search algorithm to solve optimization problems using techniques such as selection, crossover and mutation. In the Following section don't care filling using genetic algorithm is explained.

A. Solution Representation

In GA, representation of solution is called as chromosome. Our problem is to assign 0 or 1 to don't care bits in a test pattern. So the solution is represented using binary values. The don't cares of one test pattern is filled at a time. Test patterns with don't care bits generated by the tool Tetramax are taken for the experimentation.For a pattern with n don't care bits, the chromosome is an n-bit vector with i^{th} entry represents the value assigned to the i^{th} don't care bit.

Initially the chromosomes (patterns) are generated randomly to act as an initial population. Two vectors (0-filling and 1-filling vectors) are added with the initial population so that the result does not degrade by the value filled by all 0's and 1's. Fitness for each pattern is evaluated.

B. Selection and Crossover

Selection is towards the patterns with higher fitness so that the resulting vector has higher fitness. That is the resulting patterns requiring less peak temperature. After selecting parents in this way crossover is used to generate two offspring from two parents.

Parametric crossover is used for crossover operation. To generate each offspring, a random number between 0 and 1 is generated. If it is greater than 0.6, the bit of first parent is set to the corresponding bit of the first offspring and the bit of second parent is set to the corresponding bit of the second offspring. Otherwise the bit of second parent is set to the first offspring and the bit of first parent is set to the second offspring. This process is repeated to generate all the bits of offspring.

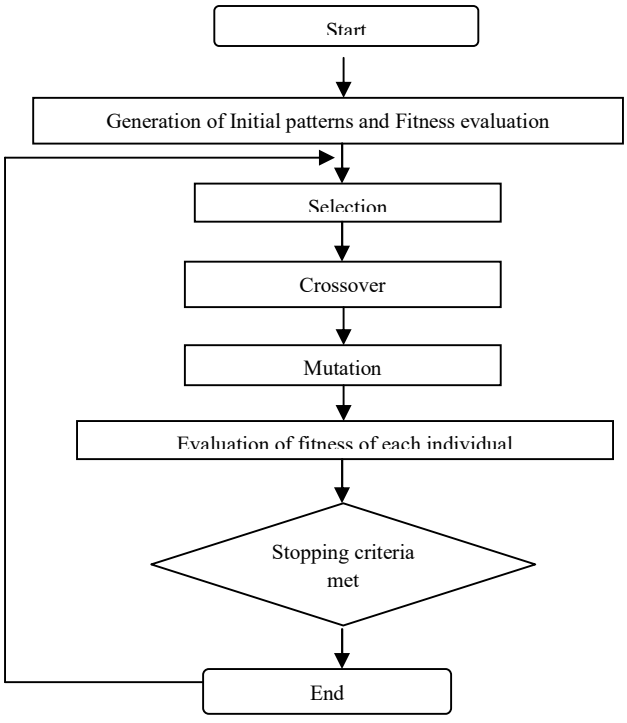

Fig.1 Flowchart of Genetic Algorithm

Flow chart of genetic algorithm is given in Fig.1.

C. Mutation

Mutation is to prevent the solutions falling into local optimum. For mutation, a random number between 0 and (n-1) is generated. The corresponding bit in the position of the random number is toggled. That is, if the bit is 0 then that is changed to 1. If it is 1 then that is changed to 0.

This process is repeated until stopping criteria is met. Here the GA is evolved with no improvement for 30 iterations.

VI. Results And Discussions

In this section experimental results of thermal aware don't care filling algorithm are discussed.

A. Schematic view of s27 circuit

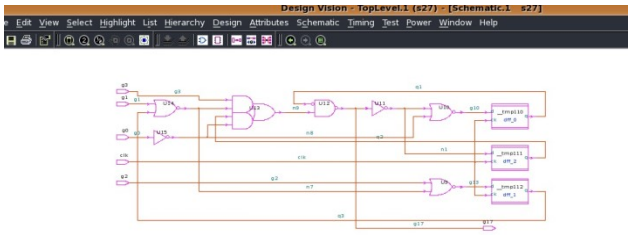

Fig.2 Schematic view of s27

The above Fig.2 shows the Schematic view of S27 benchmark circuit obtained from Design Vision tool.

B. Schematic view of s27 after inserting scan chain

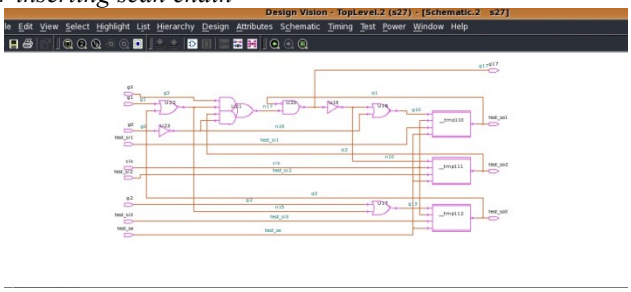

Fig.3 Schematic view of s27 after inserting scan chain

Fig.3 shows the schematic view of s27 benchmark circuit after inserting the scan chain which is obtained from Scan mode compilation of Design Vision tool. The flipflops present in the original circuit is now converted into scan flipflop.

C. Floorplan of s27

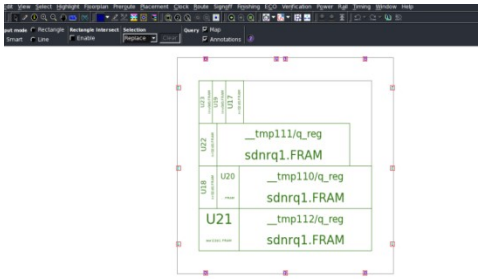

Fig.4 Floorplan of s27

The above Fig.4 shows the created floorplan of S27 circuit from the IC_compiler of Synopsys.

Patterns with don't care bits are generated using Tetramax ATPG (Automatic Test Pattern Generator) tool. 1-filling, 0-filling and MT-Filling Techniques are applied to the test pattern set. Test set with minimum temperature is given to the algorithm.

D. Total Power comparison of s27 before and after applying algorithm

Table 1 shows the power comparison of total power consumption before and after applying the thermal aware don't care filling algorithm. From the table it is observed that the power is reduced 15.61% from the power before applying the algorithm.

TABLE I TOTAL POWER COMPARISON OF S27

	Before applying algorithm	After Applying algorithm
Power(uW)	123.193	103.954

E. Peak Power of each module in s27 before applying algorithm

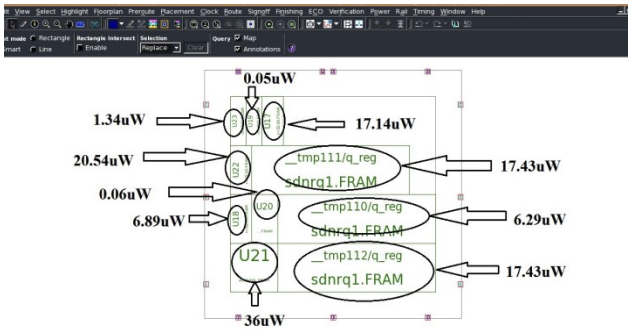

Fig. 5 Peak power of each module in S27 before applying algorithm

In Fig.5 the peak power of each module by applying 0-filling is shown. It is the power of each module before applying algorithm.

F. Peak Power of each module in s27 after applying algorithm

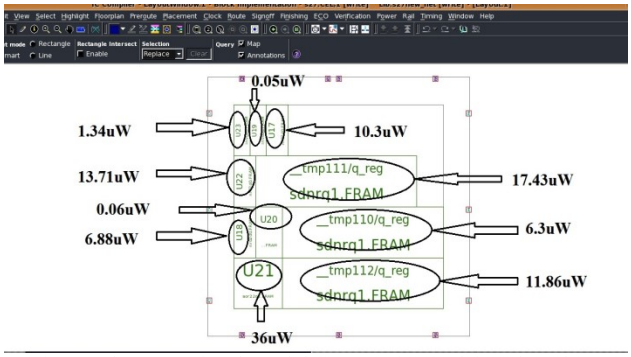

Fig.6 Peak power of each module in S27 after applying algorithm

Fig.6 shows the peak power of each module after applying the thermal aware don't care filling algorithm. From the figure it is observed that the peak power of u22, u17 and tmp112 modules are reduced which contributes to the Hotspots.

VII. CONCLUSION

Thermal aware don't care filling algorithm was used to fill the don't care bits in the Test pattern set and the algorithm was applied to the s27 benchmark circuit. The results obtained from the algorithm was compared with the other don't care filling techniques. Peak power of the modules before and after applying the algorithm was compared. Reduction in total power was 15.61 % and the peak power of the modules which contributes to the HotSpot was reduced. In future the genetic algorithm will be applied to fill don't care bits in the test pattern set.

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