DC-DC Switching Converter with Single Switch and Constant Output Based on Luo Topology

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Abstract: An ultra-high step-up, non-isolated DC–DC converter with a continuous input current was developed as a result of this research. This converter's architecture consists of a voltage multiplier cell (VMC), a positive output super lift Luo converter (POSLLC), and a quadratic boost converter (QBS) (also referred to as a cascaded boost topology (CBT)). Thus, the bold points of the topologies mentioned earlier enhance the voltage gain of the proposed topology.It is important to note that when the duty cycle is at 50%, the converter attains a voltage gain of ten. Additionally, the constant input current of the topology reduces the current stress on the input filter capacitor. This converter's topology was investigated and studied under various operating conditions: ideal and non-ideal modes, as well as continuous and discontinuous current modes (CCM/DCM). The converter's efficiency and voltage gain werealso compared to those of newly proposed converters. PLECS and MATLAB software tools were used in the investigation of the proposed topology. A 200 V/200 W prototype was constructed. The experimental results validated the theoretical study and the simulation results. The extracted efficiency was 96%.

INDEX TERMS: DC–DC converters; high gain converters; non-isolated DC–DC converters.

I. INTRODUCTION

There are two basic topologies for DC–DC converters: isolated and non-isolated types. The isolated types use a high-ratio high- frequency transformer to boost the voltage gain of the converter. Furthermore, the transformer makes galvanic isolation between the source and the load and therefore better safety than the non-isolated converters. However, using transformers increases the current stress on the switches and necessitates snubbers, which adds to the complexity, EMI noises, volume, and bulk. As a result, non-isolated converters are a better alternative when theload does not need to be isolated from the source. Theoretically and in an ideal case, the simple boost converter can increase its input voltage for all duty cycle values.However, in practical and non-ideal cases, high-duty cycle values dramatically reduce the efficiency and increase the voltage/current stresses on semiconductors. It is important to know that the diode's reverse recovery time prevents the diode from being quickly triggered. Consequently, the high-duty cycle is not appropriate for increasing the voltage gain in a simple boost converter.Therefore, other boost topologies are required for high step-up converters. Other traditional structures that address some of the drawbacks of the boost converter are the Cuk, SEPIC, and Zeta converters.
While the Cuk converter offers continuousinput and output currents, the SEPIC converter only offers a continuous input current, and the Zeta topology offers a continuous output current. However, whenemploying a moderate duty cycle, these converters are unable to increase the voltage gain

Given the aforementioned rationale, the optimal duty cycle should be around 50%.Thus, in this study, the various topologieswill be examined and compared at a 50% duty cycle.The CBT is a cascaded boost converter, also called a quadratic boost converter (QBC), and is one of these high-gain step- up converters. The topology of QBC is illustrated in Figure1a, it has an input block (IB-QBC) where the input inductor $L1$makes the current drawn from the source smooth. The output block (OB- QBC) is the voltage output filter. When the duty cycle is 50%, the converter provides a voltage gain of four. A ten- times voltage gain requires a higher duty cycle in this converter. The positive output super lift Luo converter (POSLLC), shown in Figure 1b, is another type of step-up converter topology with the continuous input current. Its output block (OB- POSLLC) is composed of two diodes and two capacitors. The ripples in the input current are an issue. We should mention that the voltage gain of the POSLLC is three at the 50% duty cycle. This convertercannot provide a high (i.e., ten) voltage ratio when using a lower duty cycle. The

other high gain converter's topology is a voltage multiplier cell (VMC) boost converter; the topology is illustrated in Figure 1c. The input block (IB-VMC) andthe output block (OB-VMC) are clearly shown. A voltage ratio of four is obtainedfor a 50% duty cycle, which is similar to the CBT. The input current continuity is notable, but its ripple is high.

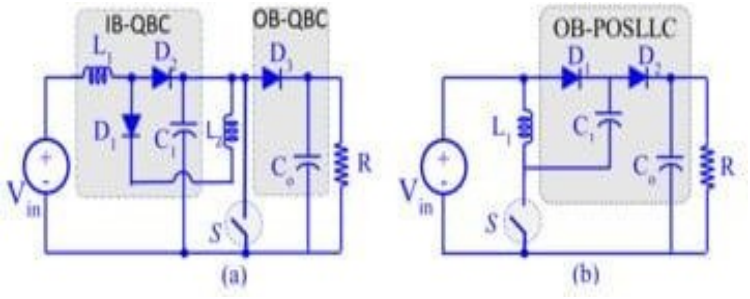

Figure 1. (a) Cascaded boost converter, Figure 1. (b) positive output super lift Luoconverter, Figure1. (c) modified form of the boostconverter by a voltage multiplier cell.

The power electronics that researchers have recommended improve topologies due to the shortages of classic topologies. Reference. combined the modified boost and POSLLC. The input current continuity remained. However, the use of POSLLC led to an input current ripple increase. The number of semiconductors is another issue in this topology. In other words, two switches are used (besides the three diodes). However, using two switches and more diodes decreases the converter's reliability. We should note that the driving circuits of the MOSFETs are not the same. In other words, one switch is low-sided, and the other is high-sided. A seven-time voltage gain is the result of a 50% duty cycle. The proposed topology involves a two-switch and three-diode topology. The first inductor of this topology provides the input current continuity. This topology combined the modified boost and classic buck–boost topologies. Such a combination brings the reversed polarity of the output voltage.

The voltage gain canprovide higher voltage gains besides theduty cycle increasing from 50%. Additionally, the output voltage is four times more than the input voltage, while the duty cycle is 50%. Reference proposed another two-switch–three-diode topology. It combines the modified forms of the boost and POSLL converters. The voltage gain for a 50% duty cycle is the same. Theinput current is continuous and appropriate for renewable energy applications. The lack of common ground between the input source and load is an issue in this topology. Used quadratic boost structures. Reference used two classic boost topologies. Both boost converters were stacked, and their stacked forms were combined. Such a topology lost the input current continuity. Consequently, the input filter capacitor suffers from dramatic high current stresses. Two MOSFETs and two diodes were the semiconductors used in this topology. A four-time voltage ratio was the result of a 50% duty cycle.

Reference proposed another quadratic boost topology. It increased its voltage by replacing the MOSFET of the conventional boost topology with an improved part. However, such an improved part led to a dramatically high diode voltage stress. The number of each component type was the same as in.Reference proposed another quadratic boost topology, combing boost, and Cuk topologies. The number of each component type was 2. Consequently, a low number of components were used. Thesame with, i.e., the second diode withstooda higher voltage than the output voltage. Notably, higher duty cycle percentages provided higher voltage gains in Referenceproposed a high step-up voltage gain basedon VMC and a voltage doubler cell (VDC). The base topologies of VMC and VDC (improved) are classic boost topologies. Consequently, the input currentwas continuous, and the common ground between the input source and load remained. This topology provides a six-

time voltage gain by a 50% duty cycle. Reference introduced a simple cascade connection of two boost converters and a VDC. Consequently, it could increase its input voltage to eight times more than itself, while the duty cycle is 50%. This converter uses the boost topologies in the CBT form. The authors of suggested an improved topology of POSLLC. The provided voltage gain provides a five-timevoltage gain, while the duty cycle is 50.
The input current is continuous. However,the inrush currents of capacitors have increased the input current ripple.
Reference recommended another one- switch topology. The conventional buck– boost converter is the base of this topology. Notably, a VMC was replaced with the base topology inductor. Due to base topology shortages, the input current was not continuous. Additionally, the output voltage was reversed. The duty cycle was 50%, and the provided voltage gain was 3. Therefore, the duty cycle must approach unity to provide higher voltage gains. Reference combined a VMC and VDC with a classic boost converter.

Therefore, the resulting voltage gain with a 50% duty cycle was eight times. Using VMC instead of the boost converter's inductor increased the input current ripple. Reference used two various VMCs with the conventional boost. The improved VMC was replaced with the converter's inductor. Notably, the input current ripple increased due to the mentioned replacement. Reference combined two conventional boost topologies, VMC and POSLLC. The mentioned VMC was replaced with the inductor of the first boosttopology. Consequently, the input current ripple increased. Moreover, the employed POSLLC at the second part led to another inrush current. Notably, the proposed converter in provides a 10-times voltage ratio with a 50% duty cycle. In this paper, a new topology is proposed to reach a voltage gain of 10 times at a 50% duty cycle. The composition of the proposed ultra-high step-up non-isolated DC–DC topology is depicted in Figure 2a. It is something of a cross between CBT, POSLLC, and VMC topologies, making itsuitable as a high step-up converter. The complete circuit of the proposed topologyis shown in Figure 2b. The proposed topology has the combined features of thethree topologies. The CBT or QBC topology can increase its input voltage to four times when its duty cycle is 50%.
Additionally, the POSLLC and VMC use the voltage lift technique to provide a higher voltage gain. The proposed topology is based on all three mentioned converters. CBT is the fundamental part ofthe proposed converter, and its various blocks have been improved by incorporating the POSLLC, which replaces the output block of the CBT (OB-QBC). Inthis case, there are two choices to use the VMC: (1) the VMC substitutes the inductor $L1$ or $L2$ of Figure 2a. Substituting $L1$ will increase the input current ripples while substituting the inductor $L2$ leads to an increase in the voltage gain and continuity of the input current. The proposed topology is therefore based on the latter approach (see Figure 2b), which employs a double voltage lift technique, allowing for a very high-voltage gain while ensuring input current continuity and small ripples.

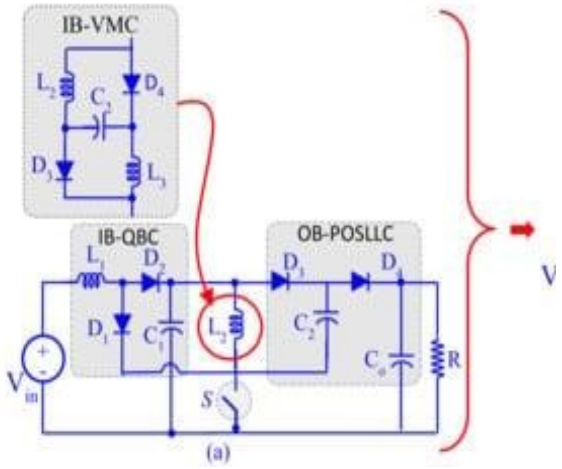

Figure 2. (a) The composition of theproposed converter,

Ideal and Continuous Current Mode of Converter

The proposed new topology of DC–DC converters is capable of providing a ten- times voltage ratio at a 50% duty ratio. Asthe front part is a CBT (see Figure 2a), thesuggested converter draws a constant current from the source. As a result, the difficulties in the input filter design are overcome. Figure 2b illustrates the complete topology of the present converter, which is implemented by cascading a CBT, POSLLC, and VMC. In other words,

this topology is a modified form of CBT. Note that the VMC has beenplaced instead of POSLLC's inductor. In the second step, the modified POSLLC is replaced with the second inductor of CBT (Figure 2a). Therefore, the voltage ratio ofthe topology increased, and the bold features of CBT remained. Notably, this converter was designed for a continuous current mode (CCM). Moreover, the extracted relations during this section are appropriate for the ideal mode.The activation of the first switch starts the first operating mode. Due to the activationof the switch, the first, third, fourth, and fifth diodes are activated. All inductors are magnetized by their positive voltages during this operating mode.

II. SIMULATION AND EXPERIMENTALRESULTS

This section presents the simulation and experimental results to validate the theoretical analysis. PLECS software tools were used to simulate the proposed converter. Such software is suitable for power electronics and control projects.Simulation results were obtained using realistic assumptions. Moreover, the energy-storing components had to be determined using functional constraints, such as input voltage, the duty cycle, the output current, the current ripple of inductors, and the voltage ripple of capacitors. The input voltage was 20 V, which was defined by the equipment limits. In addition, the switching frequencyof MOSFET was 50 kHz due to the frequency limits of employing the wires of the inductors. Moreover, the power quality considerations defined 30% and 5% as the current ripple of the inductor and the voltage ripple of the capacitor,respectively. As mentioned before, the duty cycle was 50%, with an equal energy-storing/releasing time and provided suitable operating conditions; moreover, (1) expresses the average current of theinductor and average voltage of the capacitor.

$-VC_1 = VC_2 = VC_3 = 40$ V, $VC_0 = 200$ V$IL_1 = 10$ A, $IL_2 = IL_3 = 2$ A (1)

Using the calculated average voltages/currents (besides the specified current/voltage ripples) gives the following inductors and capacitors in (2).

$-L_1 = 66.6$ µH, $L_2 = L_3 = 666.6$ µH

$C_1 = 40$ µF, $C_2 = C_3 = 10$ µF, $C_0 = 1$ µF (2)

Using the parameters in (2) gave the simulation results depicts the inductor current, the capacitor voltage, and the semiconductor current wave- forms. Additionally, shows the inductor voltage, the capacitor current, and the semiconductor voltage. According to the inductor current and capacitor voltage waveforms, their average values are as in(3).

$-VC_1 = 40$ V, $VC_2 = 38.5$ V, $VC_3 = 39$ V,$VC_0 = 196$ V

$IL_1 = 10$ A, $IL_2 = IL_3 = 2$ A (3)

A 200 W prototype of the proposed converter was built and it is illustrated. The components' voltage/currents whichpresent the experimental results. The current waveforms of the inductors and semiconductors, besides the capacitor's voltage waveforms. Figure17shows the inductor voltage, the capacitor current, andthe semiconductor voltage waveform. The average current and voltage of inductors are given by (4).

$-VC_1 = 38$ V, $VC_2 = 37$ V, $VC_3 = 36$ V,$VC_0 = 190$ V

$IL_1 = 9.4$ A, $IL_2 = IL_3 = 1.9$A (4)

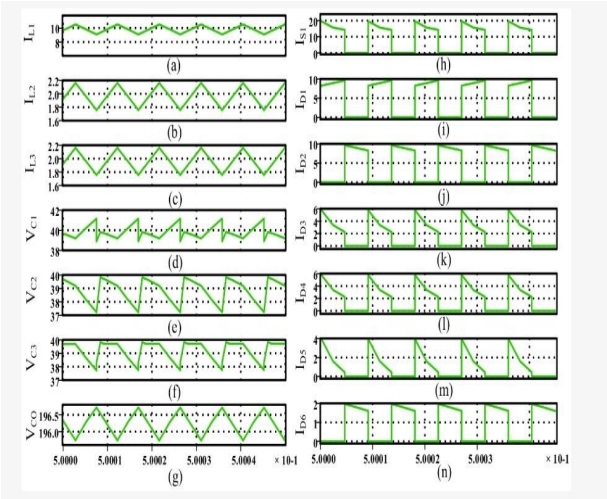

Figure 3. Simulation results: (a) first inductor current, (b) second inductor current, (c) third inductor current, (d) firstcapacitor voltage, (e) second capacitor voltage, (f) third capacitor voltage, (g) output capacitor voltage, (h)

switch current, (i) first diode current, (j) second diode current, (k) third diode current, (l) fourth diode current, (m) fifth diode current, (n)sixth diode current.

Comparing the experimental results with the simulation results and primary designconsiderations, we can see the expected difference. This discrepancy relates to thevoltage drop in the prototype's diodes.
Therefore, the voltage values are lower than the simulation results and design considerations. The average voltage of theinductors and the average current of the capacitors are zero, as assumed.

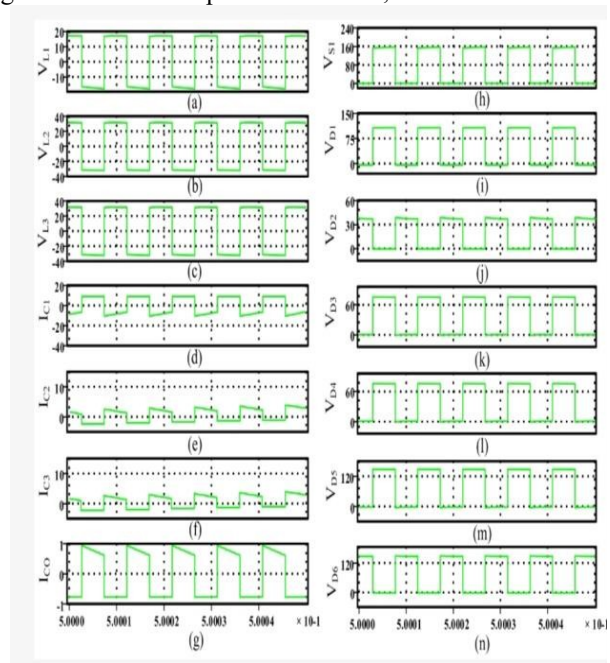

Figure 14. Simulation results: (a) first inductor voltage, (b) second inductor voltage, (c) third inductor voltage, (d) firstcapacitor current, (e) second capacitor current, (f) third capacitor current, (g) output capacitor current, (h) switch voltage, (i) first diode voltage, (j) second diode voltage, (k) third diode voltage, (l) fourth diode voltage, (m) fifth diode voltage, (n) sixth diode voltage.

The differences in the reported values stand from the average voltage in the capacitor prototype. Therefore, there is a difference in the semiconductor voltage compared to the theoretical values and simulation results. Moreover, the output voltage difference causes the contrast of the average output current. Therefore, the average currents of the inductors and semiconductors are different from the simulation/theoretical outcomes. In otherwords, there is a negligible difference.

Consequently, the corresponding figures of the E–E type have rising behaviours of wider spans. The differences in the corresponding figures regard the theoretical relations and the experimental results considering approximations.
Therefore, the higher duty cycle makes the mentioned differences appear. In Figure18, the converter's efficiency based on the theoretical equations and the experimental outcomes were extracted for the E–E, E–I, and toroid types. We should note that the E–E type of inductor requires a lower wire value to achieve inductance than the rest. Therefore, the corresponding efficiency of the E–E type provides the highest value in the theoretical/experimental outcomes. Thetoroid type needs the highest value of the wire to achieve the same inductance.
Therefore, the lowest value of the efficiency belongs to the toroid type. It isworth noting that the differences in the corresponding figures of the theoretical and experimental results were caused by neglecting some type of loss in the theoretical relation. Such an analysis was

CONCLUSIONS

This paper introduced an ultra-high step- up DC–DC converter with a continuous input current. This converter's architectureconsists of a novel combination of VMC, POSLLC, and QBC topologies. When the duty cycle is at 50%, the converter attains a voltage gain of ten. The constant input current of the topology reduces the current stress on the input filter capacitor. This converter's topology was investigated and studied under various operating conditions: ideal and non-ideal modes, as well as continuous and discontinuous current modes (CCM/DCM). The theoretical study of the proposed topology was studied for both CCM and DCM. The converter's behaviour was discussed for both the ideal and the non-ideal states of the circuit components. The proper functionality of the non-ideal case was discussed and compared with the recently suggested converter topologies.

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