Design and Performance Enhancement of Novel CNTFET over FinFET at Nano Regime

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Abstract- Developing technologies need smaller and faster IC's in order to reduce chip area, leakage power and to increase switching speed; Till recently MOSFETs were continuously scaled down to nano regime but further scaling below 45nm, MOSFET's suffers from Short Channel Effects (SCE's) which leads to degraded performance of the device. Hence designing new device structure as well as exploring novel channel materials with different gate oxide material is need of the day in the semiconductor industry. In the proposed research article, novel device structures such as FinFET and CNTFET are designed and evaluated the performance in terms of leakage and speed. FinFET performance is compared with performance of CNTFET at 14nm technology nodes. Efforts have been made here to improve the performance of these nano devices by changing the dielectric material like SiO2 by high K dielectric materials such as TiO_2 and HfO_2 in the gate oxide region of the device. So here significant reduction in leakage current with reduced dielectric thickness has been observed. Thus performance with respect to both speed and leakage is improved in both FinFET and CNTFET devices is achieved at 22nm and 14 nm technology nodes.

Keywords – **CNTFET, FinFET, MOSFET, Integrated Circuit, Short channel Effects, Nano regime.**

I. INTRODUCTION

Modern emerging sophisticated robotic and embedded systems need to meet higher demands in terms of speed, small size ICs to carry out complex and application specific tasks. It is a big challenge for the current IC industry to develop sophisticated and smart embedded systems to meet the growing demand. Therefore, to support such system development, it is very much necessary for IC industries to scale down the transistor size and explore options to increase the speed and performance in terms of power and reliability.

However, scaling of these MOSFETs has been become a challenging task for gate length less than 32nm. When gate length of MOSFET reduced below this nano regime, the planner MOSFETs increasingly suffer due to the undesirable characteristics called Short Channel Effects (SCEs) [6-9].

There are few alternatives structures like multiple gate MOSFETs called as FinFETs, gate all around devices called as nanowires and Carbon Nano Tube FETs (CNTFETs) are emerging as strong candidates for future IC industry. Hence for the advancements with technology nodes 32nm and 22nm, foundries have introduced new type of multi-gate transistors. These nano transistors have better current control over the channel. In the proposed work the two promising devices are explored, namely FinFET and CNTFET [10,14].

II. FINFET STRUCTURE MODELLING AND SIMULATIONS

FinFET can have two or more gates to have better current control over the channel. As stated earlier, FinFET with multiple fins gives the better drive current and hence FinFET with multiple fin is simulated. Simulated structure is shown in figure 2.1.

Applying gate first process, The FinFET structure is designed and developed with gate structure on both sides of the channel. The same FinFET is characterized for I-V characterizes and analysed at different node technologies in the following sections. The gate first process flow is advantages in terms of its compatibility with CMOS process [12,13]. However, gate last process is also explored to the fullest because of its thermal stability and performance

improvement with high K dielectric materials as discussed in following section.

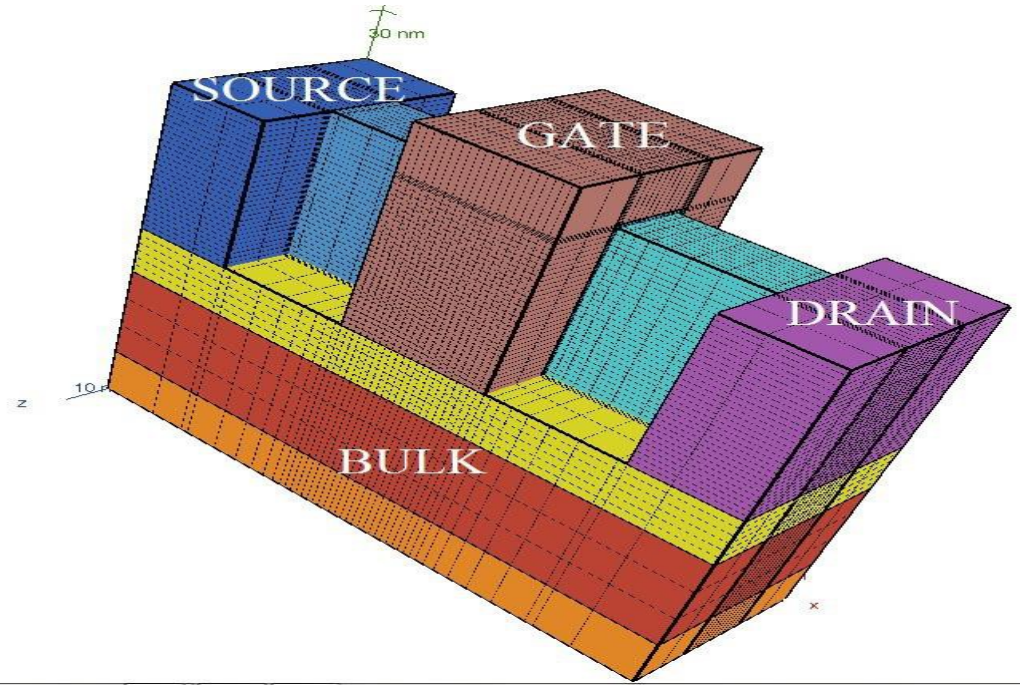

Figure: 2.1 Modelled FinFET device structure

As an alternate device structure Carbon Nano Tube FET is a explored to improve performance in terms of speed and power.

When above said modelled nano transistor is evaluated for performance in terms of its speed and leakage current, it is found that the FinFET structure overcomes the short channel effects faced in the MSOFET at nano regime specifically below 45nm up-to 14nm.

III. CARBON NANO TUBE MODELLING AND SIMULATION

Device simulation is carried out using Tiber cad tool. Here first step is to model the device and generate suitable mesh grid. This is achieved with Gmsh program or DEVISE module of ISE-TCAD. Here device modelling is carried out using Gmsh, where model is designed using bottom up approach. Once all regions of the device are formed, next step is to develop a mesh file of the device. The density of mesh elements over entire device can be controlled by properly defining the characteristic mesh length value in every point of device. Thus smaller the value of characteristics mesh length, more is the mesh density close to that point. CNTFET modelled with top gate is as shown in fig 3.1

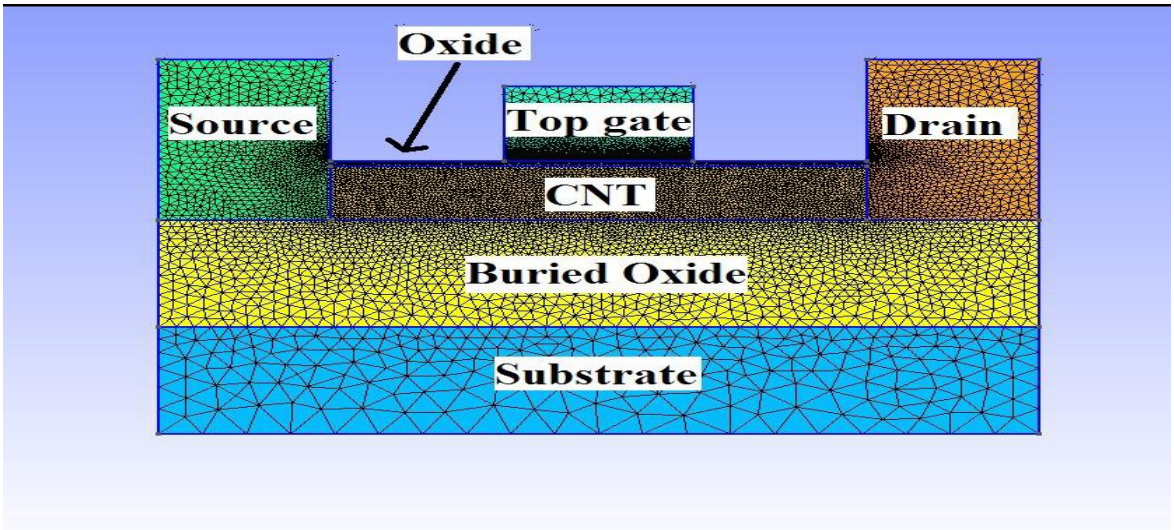

Figure: 3.1 Modelled of CNTFET device showing all regions

IV. RESULTS AND DISCUSSIONS ON DEVICE CHARACTERISTICS

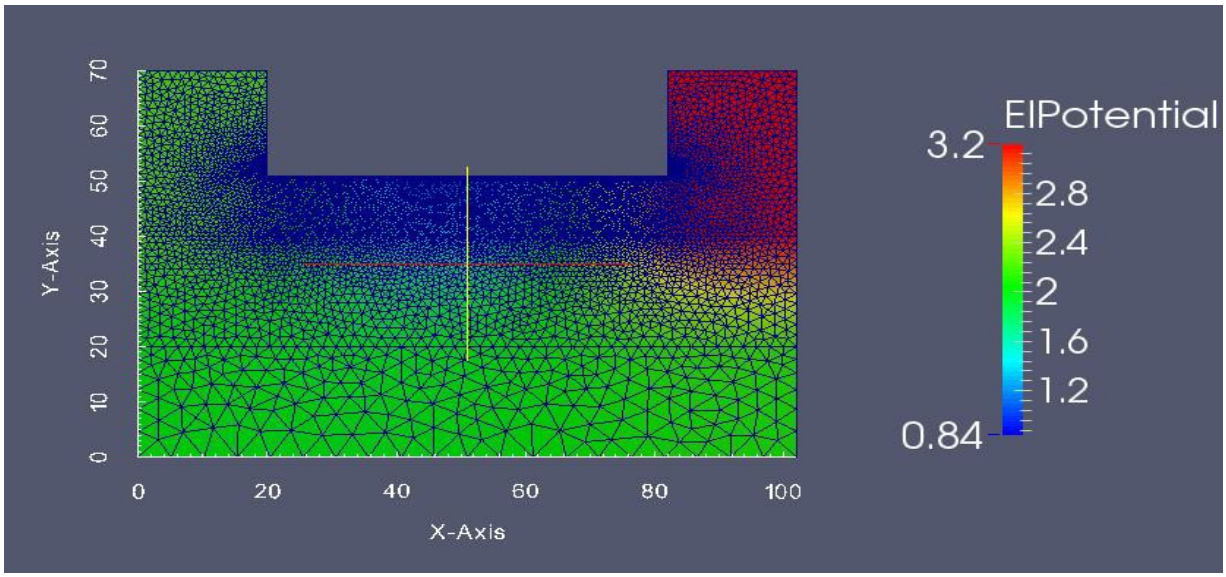

Figure 4.1**:** Electrostatic potential of CNTFET observed at **ON** state

From the graph of electrostatic potential of CNTFET in the ON state gives clear indication that the potential is very minimal at around 1 along the channel. The value of electrostatic potential is uniform throughout the buried oxide layer and the substrate, through the source.There is a surge in the Electrostatic potential at the Drain terminal.
The Electrostatic potential of CNTFET in OFF state and observations from the below graph is made here.

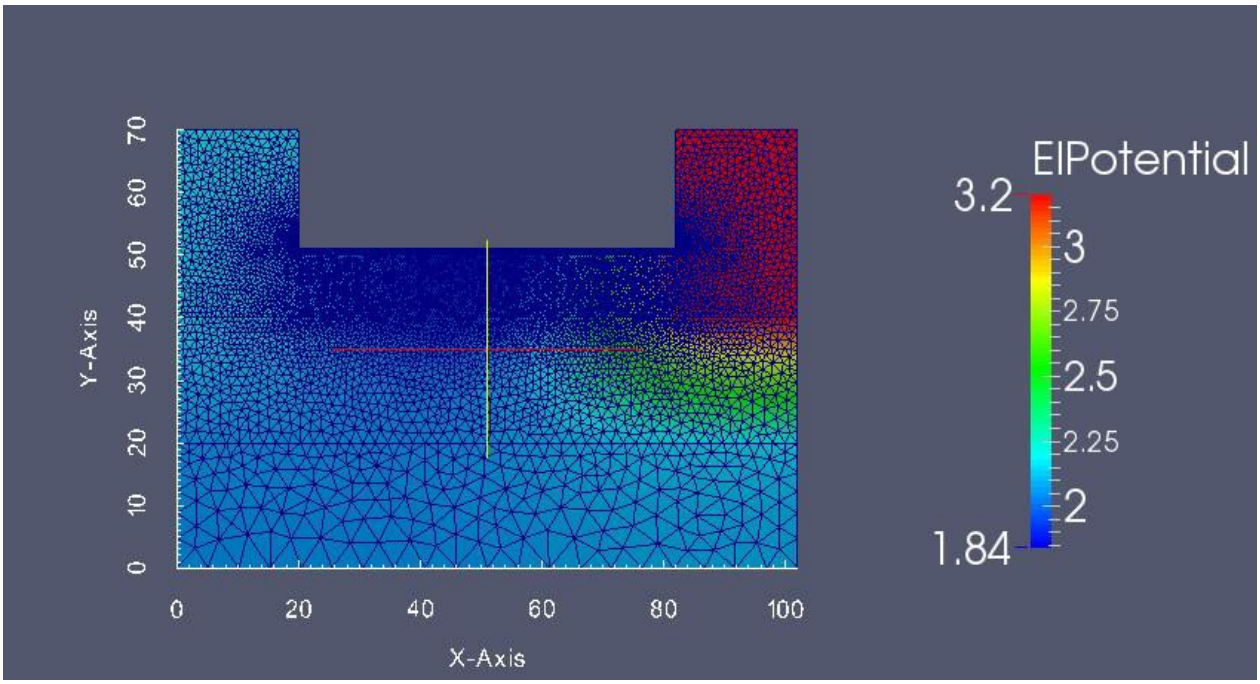

Figure 4.2**:** Electrostatic potential of CNTFET observed at **OFF** state.

When the device is in OFF state, the electrostatic potential is constant throughout the device except for the drain Terminal. At the drain terminal it is of the highest observed magnitude. A small Stray leakage can however be noted at the Buried oxide layer near the Drain terminal

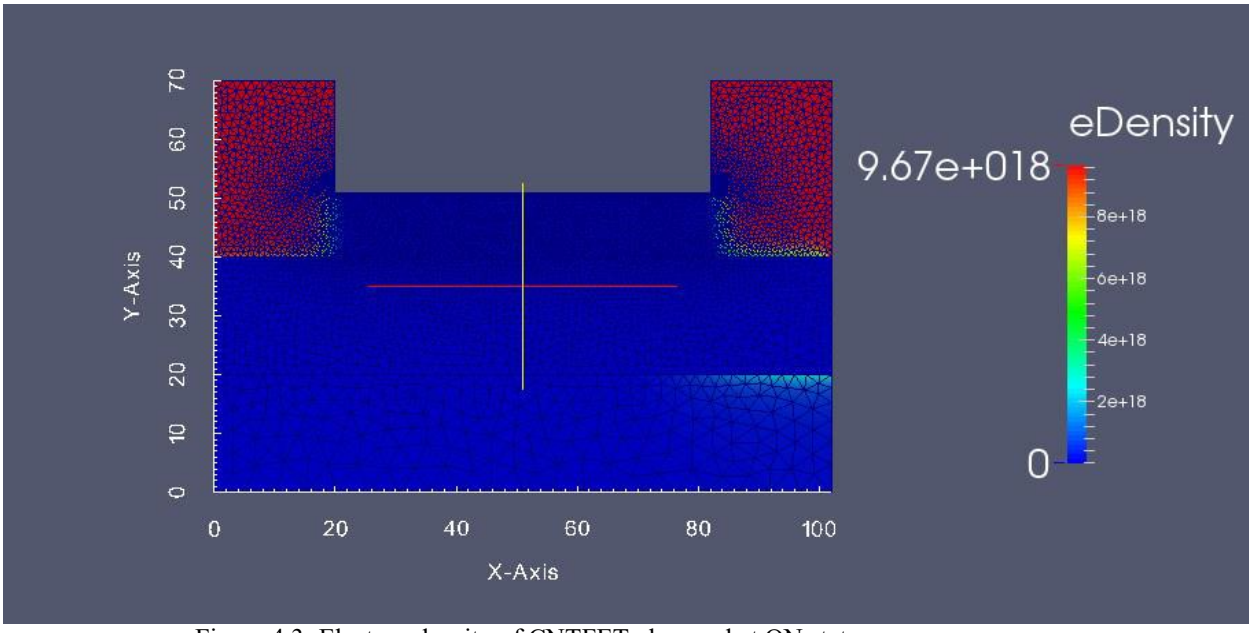

Figure 4.3: Electron density of CNTFET observed at ON state

When the device is in ON State, the electron density is uniform throughout the Substrate material and the Buried oxide layer. Although a small stray leakage can be noticed near the drain end between the junction of Oxide layer and substrate, which is not the highest in magnitude but comparatively more. Electron density is almost the same

throughout the CNT as it is throughout the substrate and buried oxide layer. The density however surges to maximum at the Source and Drain terminals with both the ends having maximum density.

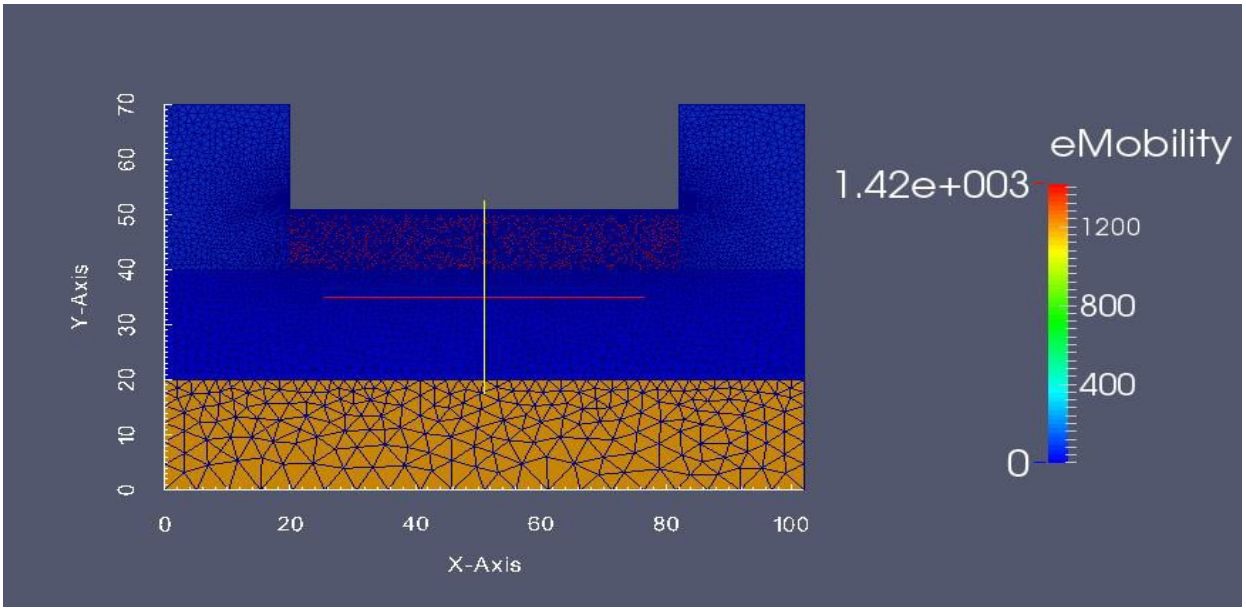

Figure 4.4: Electron mobility of CNTFET observed at ON state.

When the device is in ON State. The mobility of electrons is nearly perfect i.e., uniform throughout the device. This means fabrication / design engineers now don't have to worry about any accidental failures due to malfunction. This also shows that they are very accurate devices and hence can replace traditional FETs in terms of Speed.
From V-I characterization of CNTFET at 22nm and 14nm nodes it is clear that the on state drain current exceeds in CNTFET compared to current in FinFET i.e., with low K dielectric also the current is higher in CNTFET than FinFET due to Carbon Nano Tube property that current conduction is higher than silicon. Again with use of high-k dielectric material (HfO_2), the on state current improves further and the I_{on}/I_{off} ration also improves as shown in table below.

Table: Results comparison between FinFET and CNTFET

		I_{ON}/I_{OFF} Ratio	
S.No	Dielectric Constants	FinFET(14nm)	CNTFET(14nm)
1	With low dielectric constant(SiO_2)	1.06E+03	4.23E+04
2	With high K dielectric constant(HfO_2)	4.24E+05	4.56E+06

Therefore, inference is drawn here that both perform better in terms of I_{on} and I_{off} and hence I_{on}/I_{off} ratio get enhanced when compared to MOSFET device at these technology nodes. Also improvement in result indicate that the high K dielectric materials like HfO_2 and TiO_2 helps in further reducing oxide thickness and leakage(I_{off}) and hence reduced power consumption in the chip and increased processing speed of IC is possible.

V. CONCLUSION

The TCAD modeling and simulation of both FinFET and CNTFET is carried out successfully. Various simulation results show that the performance of these both devices have been achieved. FinFET gives better performance in

comparison with MOSFET in the nano regime and the leakage gets reduced due to its fin structure and high dielectric materials such as TiO2 and HfO2 used. When FinFET performance is evaluated with high k dielectric material in comparison with CNTFET device, later one outperforms at both at 22nm and 14nm technology nodes. In the interpretation of results, it is found that the leakage and switching speed of CNTFET has improved due to its carbon nano material property. This is improved further by high K material. FinFET with the channel material other than silicon has shown good results. CNTFET at 14nm node and with high K material shows 17% improvement in the ration of I_{ON}/I_{OFF} compared to FinFET at same node indicating reduced leakage and enhanced on state current of the device. The CNTFET shows the least variation to scaling and provides better performance in comparison to FinFET, hence is promising candidate for the future nano electronics and CNT based sensor development applications.

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