Four Way Traffic Light Controller System Based On Congestion And Emergency Situation

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Abstract - The traffic light control systems are mostly used to control the movement of vehicles in the road side. The project used to prevent theaccident and equally to divide the path. The existing TLC system is based on fixed time slots and does not have the any changes according to real time basis.Problem of the project is long waiting times for all routes. The proposed method using the FPGA technology to avoid the waiting time and safe driving also. This project to achieve the automatic timing system based on the density. It works under the both congestion and emergency situation such as VIP(Very Important Person) vehicle, Ambulance(Australia Medical Bureau Under Law and National Corresponding Emergencies) and Fire Engines. Here,the simulation is achieved by verilog HDL language and implemented on ALTERA DE0. Existing TLC using the microcontroller instead of this system using the CAN controller already present in FPGA kit to avoid delay. IR sensor is used in this project to detect the sound. This implementation technology show the result of duration is different for different routes. Thus the result of project to reduce the congestion and also works in emergency situation.

Keywords:Trafficlight,FPGA,verilog,CANcontroller,ALTERADE0,IRsensor.

I. INTRODUCTION

Traffic congestion is more in cities side due to number of vehicles are increasing day to day. The system used to schedule and control the traffic flows in road side using the scheduler light cycles.This system provide safe scheduling to share the road intersection in all traffic flows. The existing TLC system difficult to adopt with varies situation because it having equal time duration for all conditions in both peak and off peak hours.The previous system inefficient to both congestion and emergency situation. These problems are day by day increasing in modern cities. The proposed method efficient for both congestion and emergency situation in four road junction. In this paper, traffic light controller system designed and simulated using Altera DE0.

During peak hours the peoples are going or leave from some places like school, college and offices without traffic light system that will causing the traffic jam. In four way TLC system , time duration must be increased or decreased when many people ‘s are crossing the road and also emergency situation like Ambulance(Australia Medical Bureau Under Law and National Corresponding Emergencies), VIP(Very Important Person) vehicle and Fire Engines. In this system using the FPGA technology that has many advantages over microcontroller in terms of speed,performance and cost wise. It develops the use of digital systems, can significantly shorten the design time, decrease the number of peripheral circuits, reduce development cost and improve system reliability[2].

FPGA is also cheaper solution compared to ASIC (custom IC) design which is only cost effective for mass production [2]. FPGA is an integrated circuit that can be programmed by the user and that consist of array of identical logic cells. Instead of microcontroller we using the CAN controller.The CAN controller is used to reduce the delay and already inbuilt in the FPGA kit. It has the high data transmission speeds. CAN controller is a two wired half duplex high speed serial network technology. The VHDL can be used to explain and simulate the digital circuit operation because of that VHDL is preferred for design of FPGA. In this paper, the design of TLC is implemented by

Altera DE.0 kit and based on VHDL using QUARTUS II.

II. EXISTING METHOD

Traffic light control systems are widely used to monitor and control the movement of automobiles a t the junction of several roads. Traffic signals are essential to guarantee safe driving at road intersections and aim to

realize smooth movement of vehicles. But there is an inherent problem in the current traffic signal system. There is a lack of switching on and off of traffic signals based on the number of vehicles on the roads which results in long waiting times for vehicles on busy routes as there is uniform waiting time for all routes. So an approach is taken where different routes at the junction will have different waiting times. This project work tries to achieve the different waiting times based on the assumption that some routes have lesser traffic than other. Here the functional simulation is achieved through Verilog programming language and implemented on Xilinx 14.7.The switching of different traffic lights through several states is achieved through Moore state diagram .The design is implemented on Spartan 6 family. The implementation results show that duration for which green light is on is different for different routes. Thus the traffic congestion can be reduced as the vehicles on the route with the greater vehicle density will not have to wait for a longer duration for the routes with lesser vehicle density[1].

In the highly populated world, controlling of traffic is problematic. In this paper, perception of Automated day-night Traffic Light Controller system (ATLC) for attaining automatic control of road traffic flow is discussed. Here the most established efficient system called as fixed cycle method is employed with peak and off-peak time slots. The proposed method will be efficient for reducing the waiting time during the off peak slots.

This also considers an emergency and/or VIP vehicle passes and the safety of pedestrians. This system offers security and identification of breaking rules by race drivers. The low cost Automated Traffic Light Controller system provides smooth transportation and it is developed with Verilog HDL and tested using Timing Simulation. This proposed system is implemented using Wipro Mission10x UTLP Board, in which Xilinx SPARTAN 6 FPGA is mounted with additional interfaces[2].

Growing numbers of road users and the limited resources provided by current infrastructures lead to ever increasing travelling times mainly because of use of traditional traffic light controllers. The Intelligent Traffic Light Control system proposed in this paper aims at reducing waiting times of the vehicles at traffic signals. Present Traffic Light Controllers (TLC) are based on microcontroller and microprocessor. The limitation with the existing TLC is that it uses fixed time slots, which is functioning according to the program that does not have the flexibility of modification on real time basis. This proposed system makes use of FPGA technology along with traffic sensors to control traffic according to the traffic requirement and thus reduces the waiting time, at an intersection of two roads. The time intervals of the green, yellow and red states are based on real time traffic density, which optimizes traffic light timing and avoids traffic congestion, and it is an improvement upon the efficiency of the current Traffic Light Controllers. The system has been successfully tested and implemented in hardware using ALTERA Cyclone II- FPGA. The system has many advantages over the exciting TLC[3].

Traffic lights are the signaling devices used to manage traffic on multi-way road. These are positioned to control the competing flow of the traffic at the road intersections to avoid collisions. By displaying lights (red, yellow and green), they alternate the way of multi-road users. The implementation of traffic Light Controller can be through a Microcontroller, Field Programmable Gate Array or Application Specific Integrated Circuit. FPGA implementation is advantageous over ASIC and microcontroller; number of IO ports and performance compared to microcontroller and implementation with FPGA is less expensive compared to ASIC design. This paper presents the FPGA implemented low cost advanced TLC system using ChipScope Pro and Virtual Input Output. The TLC implemented is one of the real and complex signaling lights in Kingdom of Bahrain, for pedestrian way included four roads and sensors and camera assisted motorway. The system has been implemented in hardware using Spartan-3E FPGA[4].

III. PROPOSED METHOD

The existing system inefficient to both congestion and emergency situation. These problems are day by day increasing in modern cities. The proposed method efficient for both congestion and emergency situation in four road intersection. In this paper, traffic light controller system designed and simulated using Altera DE0. In four way TLC system , time duration must be increased or decreased when many peoples are crossing the road and also emergency situation like Ambulance (Australia Medical Bureau Under Law and National Corresponding Emergencies), Fire Engines and VIP(Very Important Person) vehicle. Instead of microcontroller we using the CAN controller.

The CAN controller is used to reduce the delay and already inbuilt in the FPGA kit. IR sensor is used in this project to detect the sound and also measure the congestion. Here, the simulation is achieved by verilogHDL language and implemented on ALTERA DE0 usingQUARTUS II.

a) Structure of Road:

In this paper four road structure is shown in the Fig.1. In every road side, we have to place four IR(Infra-Red) sensors and RF Modules. IR sensor to detect the vehicle, when they not follow the traffic rules.cTo identify the emergency vehicles we using the RF Modules. The direction is denoted by the arrow marks. In generally, a traffic light system has the three lights such as Red,Yellow and green.Agreen light indicate the vehicles to go in the bottom of the signal, red light indicate the vehicles to stop in the middle of the signal and yellow light indicate the vehicles to get ready to go and stop in the top of the signal.

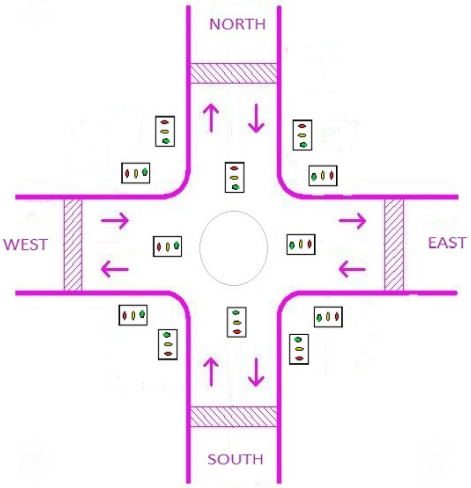

Figure 1: Four Way Road Structure

The above figure consists of twelve traffic light signal and that can be divide into two parts one is center part and another one is side part. The center part has four signal to control the movement of vehicles and side part has six signal to control the human beings to crossing the road.

In four road structure, if one road is green then other signal of road is red after some time next road is green then other signal of road is red this process is continues every day to control the traffic. If the center four signal of road is all red then the six side signal of road is all green to allow the people to crossing the road.

b) State Table:

The time duration of signal lights are shown in given Table. The time duration is increased or decreased based on the density.

State	Time in sec	C1	C2	C3	C4	S1	S2	S3	S4	S5	S6	S7	S8
Initial	0-5	R	R	R	R	R	R	R	R	R	R	R	R
West 1	Infinite	Y	R	R	R	R	R	R	R	R	R	R	R
West 2	5-25	G	R	R	R	R	R	R	R	R	R	R	R
West 3	25-30	Y	R	Y	R	R	R	R	R	R	R	R	R
North1	30-50	R	R	G	R	R	R	R	R	R	R	R	R
North2	50-55	R	Y	Y	R	R	R	R	R	R	R	R	R
East 1	55-65	R	G	R	R	R	R	R	R	R	R	R	R
East 2	65-70	R	Y	R	Y	R	R	R	R	R	R	R	R
South1	70-95	R	R	R	G	R	R	R	R	R	R	R	R
South2	95-100	R	R	R	Y	Y	Y	Y	Y	Y	Y	Y	Y
Pedestrains	100-120	R	R	R	R	G	G	G	G	G	G	G	G

c) State Diagram:

The graphical representation of traffic light control system is shown in figure in the form of state diagram which is given below. It consists of eleven state and give twelve operation of light signal.

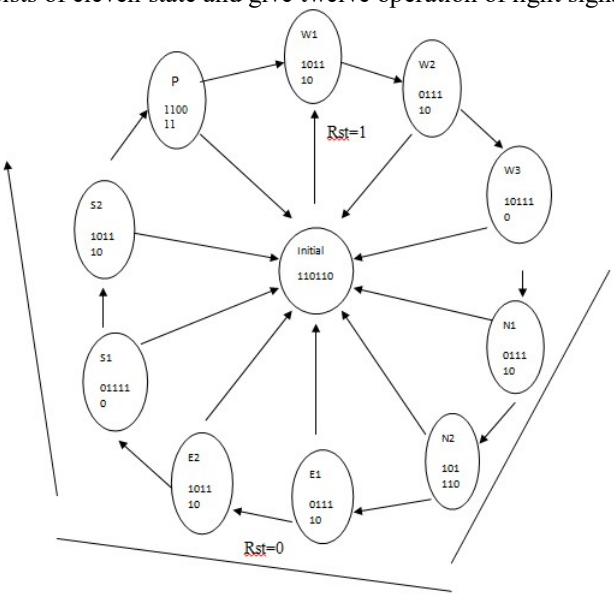

Figure 2: state diagram for four road junction

d) Algorithm:

Step 1: start

Step 2: Initial stage of TLC, all lights c1-c4 and s1-s6 are ON condition of red signal.

Step 3: First 5secs, c1 is ON of yellow signal after c1 is ON condition of green signal upto 20secs and remaining are red signal. Step4:Next c1and c3 is ON condition of yellow signal upto 5secs after c3 is ON condition of green signal then c1 and remaining are red signal upto 20 secs.
Step 5:Next c3 and c2 is ON condition of yellow signal upto 5secs after c2 is ON condition of green signal then remaining are red signal upto 10secs.
Step 7:Next c2 and c4 is ON condition of yellow signal upto 5secs and c4 is ON condition of green signal then c2 and remaining are red signal upto 20secs.
Step 8:Next c4 and P is ON condition of yellow upto 5secs after p is ON condition of green signal then c4 and remaining are red signal upto 20secs.
Step 9: End

IV. BLOCK DIAGRAM OF DE0

Figure 3.gives the block diagram of the DE0 board. To provide maximum flexibility for the user, all connections are made through the

Cyclone IIII FPGA device. Thus, the user can configure the FPGA to implement any system design.

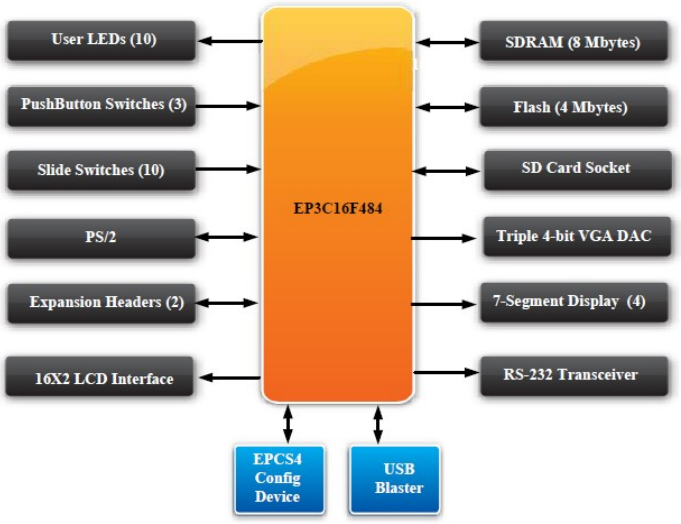

Figure 3. Block diagram of the DE0 board.

V.Hardware Implementation

The figure shows basic traffic light controller operation using FPGA kit of ALTERA DE.O. The design of our traffic light system went through different stages. The first stage was the implementation of the state diagram. The second stage was writing the VHDL code. The third stage was simulating the VHDL code.

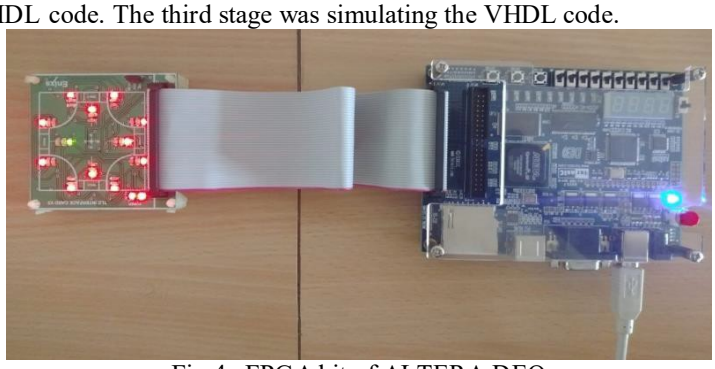

Fig.4 FPGA kit of ALTERA DEO

The fourth stage was programming the FPGA and the last stage was the development of the interface circuit. The design has been tested on ALTERA Cyclone II- FPGA [3]. In four way TLC system, time duration must be increased or decreased based congestion and emergency situation. In this system, we using the IR sensor to detect the sound and also measure the congestion. Instead of microcontroller we using the CAN controller. The CAN controller is used to reduce the delay and already inbuilt in the FPGA kit.

The simulation result of TLC is given above. If thecongestion at west side is ON condition of green signal then other sides are red. If congestion at north side is ON condition of green signal then the other sides are red. If the congestion at east side is ON condition of green signal then the other sides are red. If the congestion at south side is ON condition of green signal then the other sides are red. If all signals of four sides are red then the pedestrian is ON condition of green signal.

VI. CONCLUSION

FPGA Design of TLC with four road traffic lights has been simulated using Quartus II, implemented and tested using ALTERA DE0 FPGA kit. Over the existing method the waiting time of congestion period is reduced and also congestion situation. Instead of micro controller we using the CAN controller to reducing the delay. IR sensor is used to detect the sound and also density. Main advantage of this project time duration is increased or decreased

based ondensity and also emergency situation.

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