Design And Implementation Of High Speed Carry Skip Adder Using Carry Select Adder

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Abstract - Adders are the fundamental building blocks of any processor. In designing the adder carry generation is the critical path. There are many types of adder such as Ripple Carry Adder (RCA), Carry Select Adder(CSLA),Carry Skip Adder(CSKA) and Carry Look Ahead Adder. A Carry-Skip Adder (also known as a carry-bypass adder) is an adder implementation that improves on the delay of a RCA with little effort compared to other adders. Further to reduce the delay involved with the RCA, we replace the portion of RCA with the CSLA. Because, CSLA is the fast adder used in many data path applications, thus it reduces the carry propagation delay by independently generating multiple carries and then select a carry to generate the sum.

Keywords : Carry Select Adder, Ripple Carry Adder, Carry Skip adder.

I. INTRODUCTION

Adders are most important in VLSI designs and it is used in computer, in multipliers, in high speed integrated circuits and in digital signal processing. An adder is the basic component of an arithmetic unit. Several adders have been used in complex digital signal processing systems. General types of adder are Ripple Carry Adder, Carry Look Ahead Adder, Carry Save Adder, Carry Skip Adder and Carry Select Adder. In the digital system, the speed of addition depend on the propagation of carry which is generated sequentially after the previous bit has been summed & carry is propagated into the next position. Ripple Carry ``Adder is composed of many cascaded single-bit full adders. The circuit is simple and area- efficient but computation speed is slow. Carry Look-Ahead Adder derives faster results but there is increase in area. In carry select adder, N bit adder is divided into M parts. Each part of adder is composed of two ripple carry adders with Cin=0 and Cin=1 respectively. According to the logic state of input carry, we can select the output result by using a multiplexer. Thus, CSLA can compute faster because current adder=1respectively. According to the logic state of input carry, we can select the output result by using a multiplexer. Thus, CSLA can compute faster because current adder stage does not need to wait for the previous stages carry-out signal. In CSLA, carry propagation delay can be reduced as compared with RCA. Therefore, Carry select adder is used because it is faster than other adders and also there is further scope to reduce the area and power consumption. To, make the carry skip adder more efficient the ripple carry adder block has been replaced by the carry select adder.

II. LITERATURE SURVEY

a.RIPPLE CARRY ADDER (RCA):

Ripple Carry Adder (RCA) is a basic adder which works on basic addition principle. The ripple carry adder is constructed by cascading full adders (FA) blocks in series. The architecture of RCA is shown in figure. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carry-out of one stage is fed directly to the carry-in of the next stage. Even though this is a simple adder and can be used to add unrestricted bit length numbers, it is however not very efficient when large bit numbers are used. That is the sum and the output carry of any stage cannot be produced until the carry input occurs which causes a time delay in the addition process. The advantages of the RCA are lower power consumption as well as compact layout giving smaller chip area. One of the most serious drawbacks of this adder is that the delay increases linearly with the bit length. To overcome delay problem, a new adder structure is designed called Carry Select Adder (CSLA).

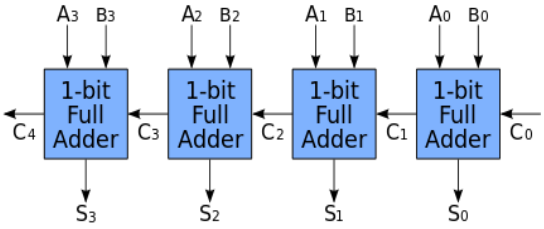

Fig.1: 4-bit Ripple Carry Adder

b. CARRY SKIP ADDER (CSKA):

A carry-skip adder consists of a simple ripple carry-adder with a special speed up carry chain called a skip chain. Carry skip adder is a fast adder compared to ripple carry adder when addition of large number of bits take place; carry skip adder has O(√n) delay provides a good compromise in terms of delay, along with a simple and regular layout This chain defines the distribution of ripple carry blocks, which compose the skip adder. A carry-skip adder is designed to speed up a wide adder by aiding the propagation of a carry bit around a portion of the entire adder. Actually the ripple carry adder is faster for small values of N. However the industrial demands these days, which most desktop computers use word lengths of 32 bits like multimedia processors, makes the carry skip structure more interesting.

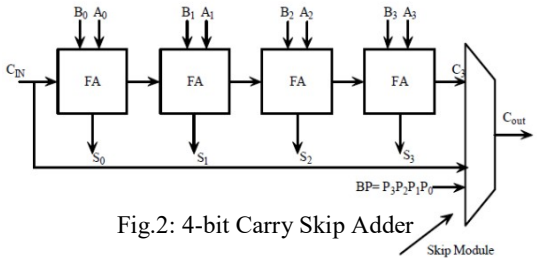

Fig.2: 4-bit Carry Skip Adder

c. CARRY LOOK AHEAD ADDER:

The carry-chain can also be accelerated with carry generate/propagate logic. Carry-look ahead adders employ the carry generate/propagate in groups to generate carry for the next block. In other words, digital logic is used to calculate all the carries at once. When building a CLA, a reduced version of full adder, which is called a reduced full adder (RFA) is utilized. Figure shows the block diagram for an RFA. The carry generate/propagate signals gi/pi feed to carry-look ahead generator (CLG) for carry inputs to RFA.CLAA is that the carry logic block gets very complicated for more than 4 bits (CLAA are usually implemented a 4-bit modules and are used in a hierarchical structure to realize adders that have multiples of 4-bits) .

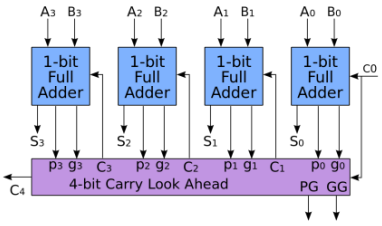

Fig.3: 4-bit Carry Look Ahead Adder

CARRY SELECT ADDER (CSLA):

The CSLA is one of the fastest adders used in many data-processing processors for performing arithmetic operations. It is also used in computational systems to alleviate the problem of carry propagation delay by generating multiple carries and then selecting a carry to generate the sum. CSLA consists of number of blocks in which RCA chains run in parallel. The principle on which CSLA works is: Two additions are performed in parallel ; blocks evaluated conditionally with carry values 0 and1. For the addition purpose RCAs are used. Therefore, CSLA uses dual RCAs structures. When the carry- in values are assigned to the blocks, then the final value is used to select the sum bits from one of the two blocks. At this point of time, carry-out values can be evaluated, which in turns selects the sum bits and carry out of the next block . In RCA, every full adder has to wait for the incoming carry before the outgoing carry is generated. But CSLA found a way to get around this linear dependency by anticipating both the possible values of carry i.e. 0 and 1 and evaluates the result in advance .Once the real value of carry is known, result can be easily selected using the multiplexer stage. Figure shows the 4-bit CSLA which consists of two RCAs in each block, one for Cin=0 and other for Cin=1.

In general, we can write the algorithm as:

If Carry in=1, then the sum and carry out are given by, Sum (i) =a(i) xor b(i) xor '1'.

Carry (i+ 1)= (a(i) and b(i)) or (b(i) or a(i)).

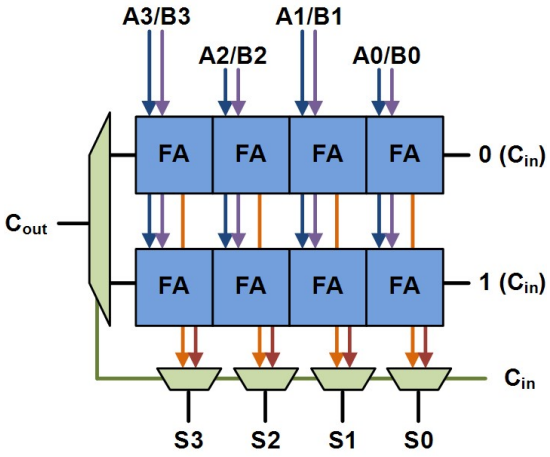

Fig.4: 4-bit Carry Select Adder

If Carry in =0, then the sum and carry out are given by, Sum (i) = a (i) xor b (i).

Carry (i+ 1) = (a (i) and b (i)).

16-BIT CARRY SELECT ADDER:

A 16-bit carry select adder can be developed in two different sizes namely uniform block size and variable block size. Similarly a 32, 64 and 128-bit can also be developed in two modes of different block sizes. Ripple-carry adders are the simplest and most compact full adders, but their performance is limited by a carry that must propagate from the least-significant bit to the most-significant bit. The

various 16, 32, 64 and 128-bit CSLA can also be developed by using ripple carry adders. The speed of a carry-select adder can be improved upto 40% to 90%, by performing the additions in parallel, and reducing the maximum carry delay. Fig, shows the structure of 16-bit CSLA. It includes many ripple carry adders of variable sizes which are divided into groups. Group 0 contains 4-bit RCA which contains only one ripple carry adder which adds the input bits and the input carry and results to sum [3:0] and the carry out. The carry out of the Group 0 which acts as the selection input to mux which is in group 1, selects the result from the corresponding RCA (Cin=0) or RCA (Cin=1). Similarly the remaining groups will be selected depending on the Cout from the previous groups.

In CSLA, there is only one RCA to perform the addition of the least significant bits [3:0].The remaining bits (other than LSBs), the addition is performed by using two RCAs corresponding to the one assuming a carry-in of 0, the other a carry-in of 1 within a group. In a group, there are two RCAs that receives the same data inputs but different Cin. The upper adder has a carry-in of 0, the lower adder a carry-in of 1. The actual Cin from the preceding sector selects one of the two RCAs. That is, as shown in the Fig, if the carry-in is 0, the sum and carry-out of the upper RCA is selected, and if the carry-in is

1, the sum and carry-out of the lower RCA is selected. According to the logic state of input carry, we can select the output result by using a multiplexer. The 64-bit, 128-bit CSLA were implemented by calling the ripple carry adders and allmultiplexers.

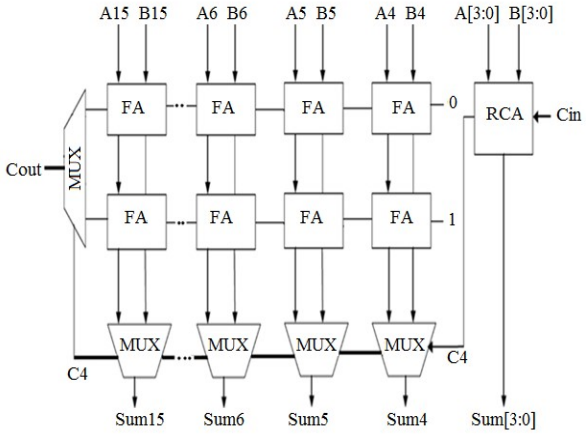

Fig.5:16-bit Carry Select Adder

64-BIT CARRY SELECT ADDER:

A 64-bit carry select adder can be developed in two different sizes namely uniform block size and variable block size. Ripple-carry adders are the simplest and most compact full adders, but their performance is limited by a carry that must propagate from the least-significant bit to the most- significant bit. The various 16, 32, 64 and 128-bit CSLA can also be developed by using ripple carry adders. The speed of a carry-select adder can be improved upto 40% to 90%, by performing the additions in parallel, and reducing the maximum carry delay. Fig shows the structure of 64-bit CSLA. It includes many ripple carry adders of variable sizes which are divided into groups. Group 0 contains 4-bit RCA which contains only one ripple carry adder which adds the input bits and the input carry and results to sum [3:0] and the carry out. The carry out of the Group 0 which acts as the selection input to mux which is in group 1, selects the result from the corresponding RCA (Cin=0) or RCA (Cin=1). Similarly the remaining groups will be selected depending on the Cout from the previous groups.
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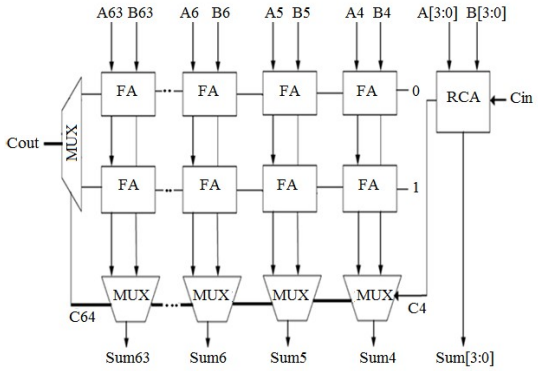
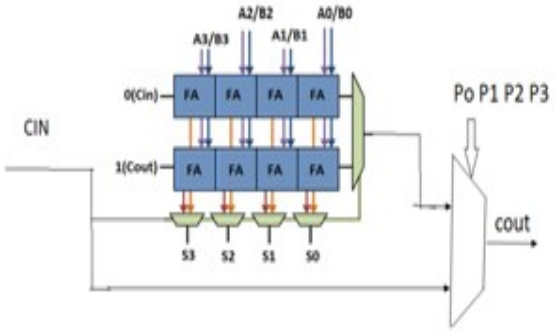


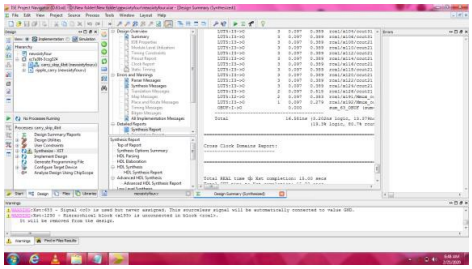
Fig.6: 64-bit Carry Select Adder

III. PROPOSED SYSTEM MODIFIED CARRY SKIP ADDER:



IV. SIMULATION RESULT

In this study, Simulation of 64 bit Modified Carry Skip Adder is implemented in Verilog HDL and logic simulation is done by using Xilinx software and the synthesis is done using Xilinx ISE 13.2



V. COMPARATIVE ANALYSIS

Existing carry skip adder versus modified carry skip adder Adder in terms of delay. It is shown in Table 1.

Table-1: Observations Carry Skip Adder and Modified Carry Skip Adder

Bits	Excisting delay in (ns)	Proposed delay in (ns)
4bit	2.094	1.724
8bit	3.061	2.888
16bit	4.956	4.802
32bit	8.831	8.721
64bit	16.609	16.581

VI. CONCLUSION

Thus we have given a clear analysis for a 64 bit carry skip adder and modified carry skip adder using XILINX ISE Tool. From the analysis it is clear that Carry Skip Adder is better than Modified Carry Skip Adder. Finally the comparative analysis of Modified Carry Skip Adder gives better performance,high speed and less delay of addition operation. In future if it is possible to reduce area and power of Carry Skip Adder using BEC-1(Binary to excess one converter) circuit.

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