Design and Implementation of High Speed Multiplier using HPM

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Abstract - Multiplier is a heavily used arithmetic operation in digital signal processing and scientific applications. With upcoming technologies, many researchers have attempted and are demanding to design high performance, low power consumption, small area implementation. Baugh-Wooley multiplication is one such scheme used for high performance. It is not widely used because of its intricate structure. In this paper, design and implementation of 8 bit Baugh-Wooleymultiplierusing High Performance Multiplier Reduction tree (HPM) technique is analyzed.

Keywords- Multiplier, Baugh-Wooley, HPM, Xilinx.

I. INTRODUCTION

Multiplication is the main source function for various multiplier . Most of the multipliers consume large area and considerable power.There are different types of multiplier, they are array multiplier ,parallel multiplier,serial multiplier, Baugh-Wooleymultiplier etc., By using array multipliers number of adders are increased due to this it consumes large area implementation. Array multipliers are well known due its structure. These are pipelined to decrease the clock period at expense latency. This multiplier uses add and shift algorithm. It has a drawback that is path delay between input and output.

Parallel multiplier is also called as binary multiplier or Braun multiplier. It has two main components are multiplicand and multiplier .In this multiplicand is multiplied by each bit of the multiplier starting from the least significant bit.Each multipliers forms a partial product , successive partial product are shifted one position to the left.The final product is obtained from the sum of the partial products .It also has a drawback that is complexity structure and delay.

This multiplier is used for signed and unsigned multiplication. Baugh-Wooley technique was developed to design direct multipliers for two's complement numbers.When multiplying two's complement numbers directly each of the

partial products to be added is signed number.Adjusts partial products to maximize regularity of multiplication array.In this paper reduction tree technique is used to design new structure of Baugh-Wooley multiplier.

II.LITERATURE SURVEY

AswathySudhakar in 2010 proposed "High Speed Power-Efficient Modified Baugh-Wooley Multipliers", in this in this they proved modified Baugh-Wooley multiplier. Here comparison of various multiplier architecture for VLSI application. The Baugh-Wooley multiplier found to be best suited for the multiplication functionality according to resolution and efficiency[6].

Andrew D. Booth present "A signed binary multiplication technique". In this a technique is described by which binary numbers of either sign may be multiplied together by a uniform process which is independent. In the design of automatic computing machines it is necessary to have two numbers whose signs are not necessarily positive[7].

III. EXISTING WORK

Baugh-Wooley multiplier is the efficient and high-speed multiplier compared with other conventional multipliers. Here the regularity of the multiplier is maximized. The Baugh-Wooley multiplier switches on signed operands with 2's complement number to make the signs of all the partial products to be positive.In digital signal processing applications multiplication in number is performed by the Baugh-Wooley algorithm.

It is the best well-known algorithm. The delay is minimized by using this algorithm and the speed is increased. By using decomposition logic method a high-speed multiplier is designed and implemented in a Baugh-Wooley algorithm. The result is compared with modified booth multiplier and Vedic multiplier. In use of different Multipliers, they applied the Baugh-Wooley algorithm and it is implemented to get the minimum delay, low power distraction and minimum area than Vedic and modified Booth multipliers[1].The two input bits given to the partial product generator to execute the scheme of both Baugh- Wooley and booth multiplier. Then it is given to the partial product reducer in carry save adder with the compressors[2].

At each side of the compressors, Half-Adders and Full- Adders are placed in a tree structure pattern for the reduction of the critical path of partial-product reducer. In the region of a vector-merging adder, the PPR sums and carries are feeds to the carry-propagate adder as a VMA implementation which gives the final result of the multiplication. In multiplier structure, the PPR structure is quite complex and therefore consumption of the power is more. The shift and add is the first and foremost operation of the PPR.

In this design the partial products are generated using shift and add operation and this is carried out in the main building blocks of a multiplier, but it is to be implemented with Half-Adders and Full-Adders. When the operands are interpreted as integers, the product is generally twice the length of operands in order to preserve the information content[3][4].

The diverting function of logic gates can be diminished by increasing the possibility of having balanced logic-zeros at the inputs, which resemble imposing more number of partial products to be equal to zero. This can be attained by bringing an enormous sum of bits which are equal to zero in the gutter of one of the two input words. In the operation, the approximations are the abode, we can feat this equity to anxiously select perpetual multiplier co-efficient to cut down the power utilization at runtime[5].

IV. MULTIPICATION PROCESS

Baugh-Wooley multiplier is the simple and well-known algorithm. In this paper objective and implementation of a conventional method for an 8-bit Baugh-Wooley multiplier and Modified HPM Baugh-Wooley has been done and compared the result with the existing multiplier . The Baugh-Wooley multiplier is a motivating implementation of a multiplier. The algorithm for 8 bit Baugh-Wooley is shown in Fig 1.

$$
\begin{array}{r}
a_7\ a_6\ \ a_5\ a_4\ \ a_3\ \ a_2\ \ a_1\ \ a_0 \\
b_7\ b_6\ \ b_5\ \ b_4\ b_3\ \ b_2\ \ b_1\ \ b_0 \\
\hline
b_0a_7\ b_0a_6\ b_0a_5\ b_0a_4\ b_0a_3\ b_0a_2\ b_0a_1\ a_0b_0 \\
b_1a_7\ b_1a_6\ b_1a_5\ b_1a_4\ b_1a_3\ b_1a_2\ b_1a_1\ b_1a_0 \\
b_2a_7b_2a_6\ b_2a_5\ b_2a_4b_2a_3\ \ b_2a_2\ b_2a_1\ b_2a_0 \\
b_3a_7\ b_3a_6\ b_3a_5\ b_3a_4\ b_3a_3\ b_3a_2\ b_3a_1\ b_3a_0 \\
b_4\ a_7\ b_4a_6\ b_4\ a_5\ b_4a_4\ b_4a_3\ b_4a_2\ b_4a_1b_4a_0 \\
b_5a_7b_5\ a_6b_5\ a_5\ b_5a_4\ b_5a_3\ b_5a_2\ b_5a_1b_5a_0 \\
b_6a_7\ b_6a_5\ b_6a_5\ b_6a_4\ b_6a_3\ b_6a_2\ b_6a_1\ b_6a_0 \\
b_7a_7\ b_7a_6\ b_7a_5\ \ b_7a_4\ b_7a_3\ b_7a_2b_7a_1b_7a_0 \\
\hline
p_{15}\ \ p_{14}\ \ p_{13}\ \ p_{12}\ \ p_{11}\ \ p_{10}\ \ p_9\ \ p_8\ \ p_7\ \ p_6\ \ p_5\ \ p_4\ \ p_3\ \ p_2\ \ p_1\ \ p_0
\end{array}
$$

Fig-1: An 8x8 bit Unsigned Algorithm of Baugh-Wooley multiplication

V.PROPOSED METHOD

Here the 8-bit Baugh-Wooley is designed and implemented by using conventional method. This Baugh-Wooley Multiplier provides an impressive implementation by using the shift and adds method with high-speed Multiplier.It is treated with straightforward multiplication for both signed and unsigned operands. Since the partial products are quite harder hence it need to be maximized for the regularity of multiplication array and lifted negative signs are used in the last stages.

The implementation of Baugh- Wooley multiplier is a frustrating implementation of a multiplier. This enables the design of a quite standard cell shape for easy manufacturing. The full adder in the multiplier design executes same number of computations, with the crosswise ripple carry propagating the input signal.The stoppage of a multiplier is determined by the number of additions to be executed. In this proposed work, the Modified HPM Baugh-Wooley multiplier has been designed and implemented.

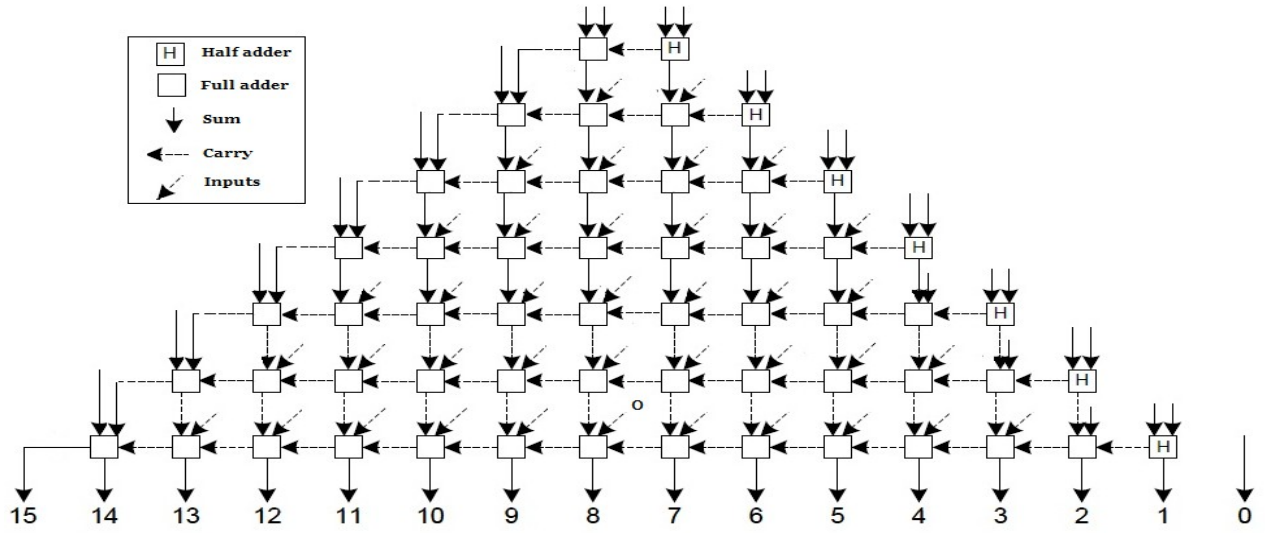

Fig -2 : Modified 8 bit HPM Baugh-Wooley

At the time of multiplication process, all the partial- products are multiplied as per the actual method in Baugh-Wooley multiplier wherein the Modified HPM Baugh- Wooley multiplier, half of the partial-products are reduced by the triangular tree pattern multiplication.

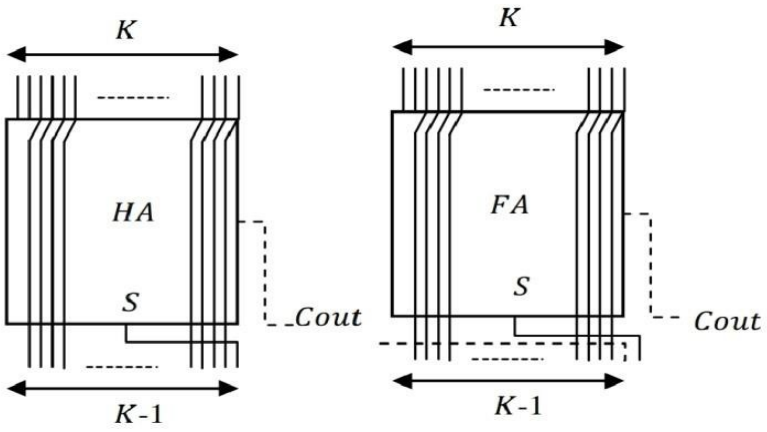

Fig-3 : HPM Half-Adder and Full-Adder Cell[1].

The triangular cell pattern has been done with the partial- products reducer, the reason for applying triangular tree pattern is to reduce the tree technique and to achieve a shorter wire length. In the sense modified means changing the structure of the adders and the HPM concept is multiplying the bits with triangular tree pattern. Thus the size of the partial-products is reduced half of the length. Therefore finally we could get the reduced delay time with high performance. The comparative analysis has been done to make sure that the Modified HPM Baugh-Wooley multiplier design is faster and performed better than other conventional multipliers[1].

VI.SIMULATION RESULTS

1.1 Simulation Results of 8 bit Conventional Baugh Wooley Multiplier Using Xilinx.

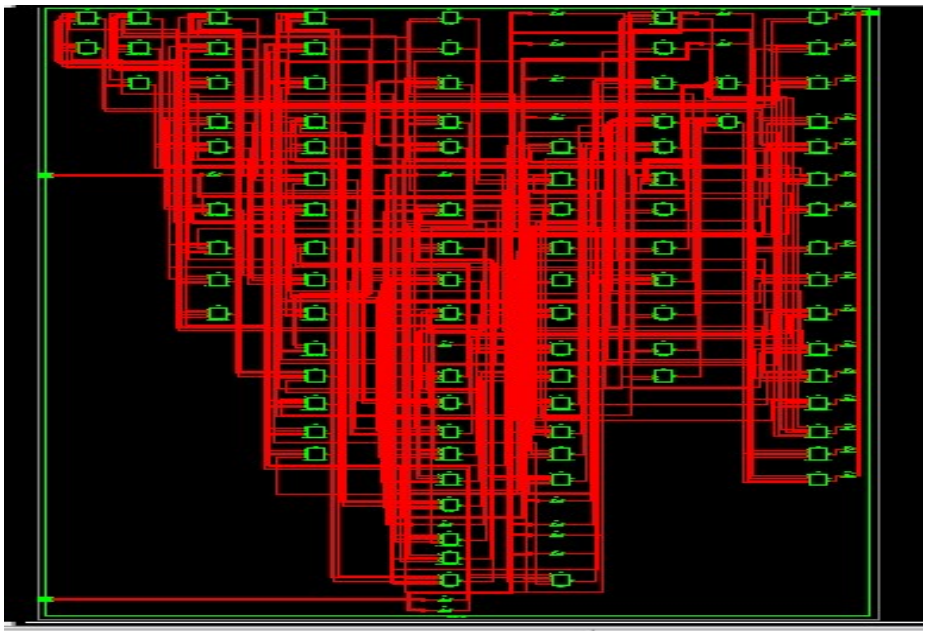

Fig-4 : RTL View of 8 bit conventional Baugh-Wooley Multiplier.

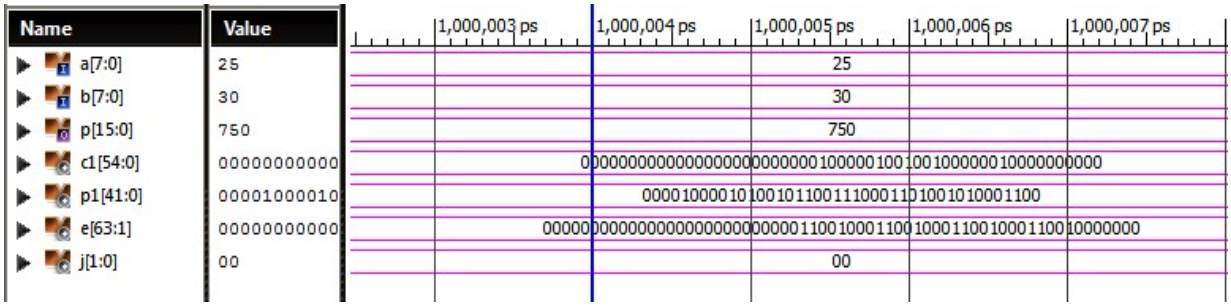

Fig-5 : Simulation result of Modified 8-bit Baugh-Wooley multiplier

1.2 Simulation Results of 8 bit Modified HPM Baugh Wooley Multiplier Using Xilinx.

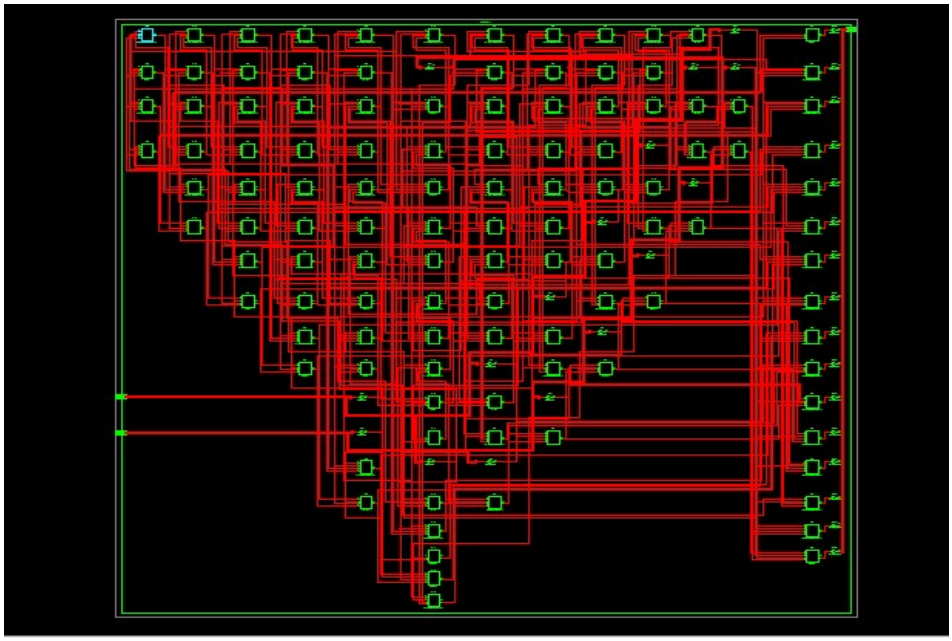

Fig-6 : View technology schematic of 8 bit Modified HPM Baugh-Wooley Multiplier.

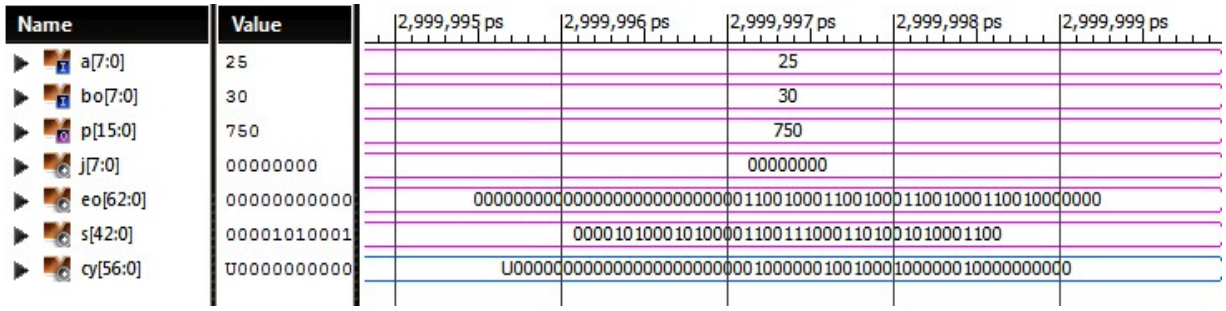

Fig-7 : Simulation result of conventional 8-bit Baugh-Wooley multiplier.

1.3RTL View of 4bitModified HPM Baugh Wooley Multiplier

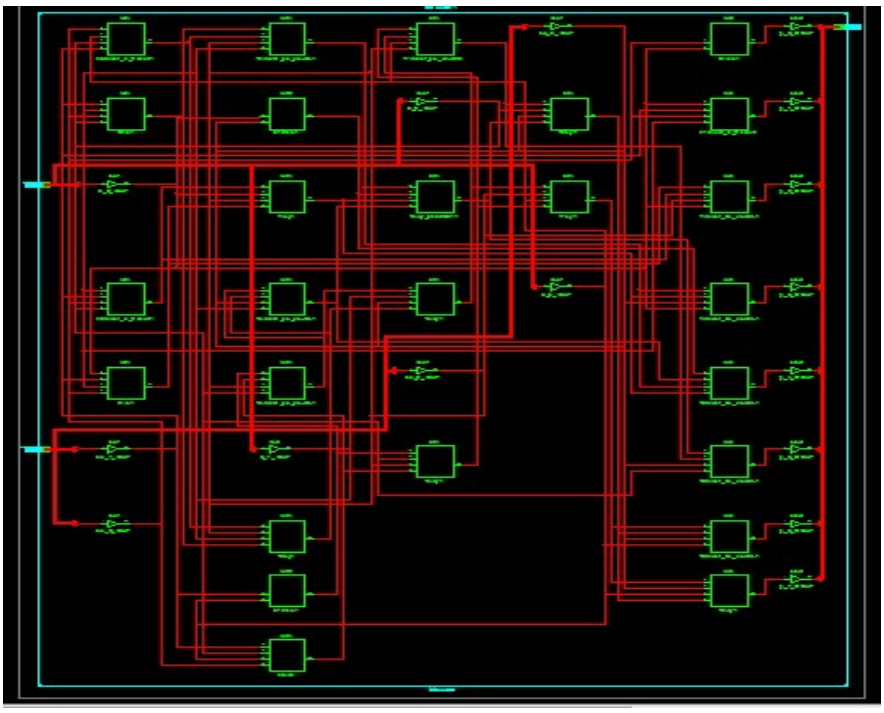

Fig-8 *RTL View of 4bit Modified HPM Baugh Wooley Multiplier*

1.4 RTL View of 4-bit Conventional Baugh Wooley Multiplier

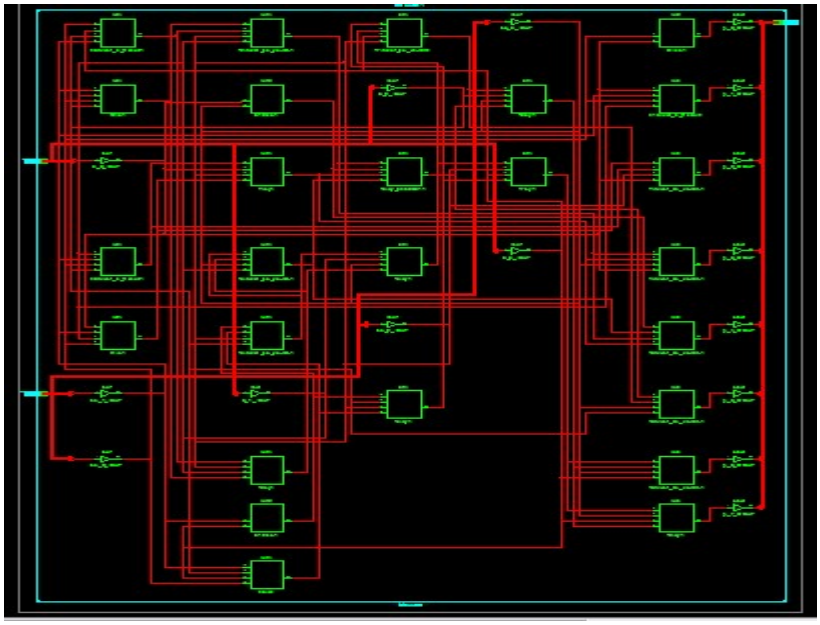

Fig-9 RTL View of 4-bit Conventional Baugh Wooley Multiplier

VII.CAMPARATIVE ANALYSIS

Both the conventional Baugh –Wooley and Modified HPM Baugh Wooley multiplier in terms of delay.

Table-1 :Observations of Conventional Baugh Wooley and Modified HPM Baugh Wooley multiplier .

Parameter	Conventional Baugh Wooley		Modified HPM Baugh Wooley	
Delay(ns)	4 Bit	8 Bit	4 Bit	8 Bit
	16.24	29.27	15.36	27.84

VIII.DEVICE UTILIZATION

Table-1 :Device Utilization Table For 4 bit Modified HPM Baugh-Wooley Multiplier

Logic Utilization	Used	Available	Utilization
Number of slices	14	14	100%
Number of 4 LUTs	20	1,536	1%
Number of bonded IOBs	16	124	12%

Table-2:Device Utilization Table For 8 bit Modified HPM Baugh-Wooley Multiplier

Logic Utilization	Used	Available	Utilization
Number of slices	58	768	7%
Number of 4 LUTs	114	1,536	7%
Number of bonded IOBs	32	124	25%

Table-3 :Device Utilization Table For 4 bit Conventional Baugh-Wooley Multiplier

Logic Utilization	Used	Available	Utilization
Number of slices	17	768	25%
Number of 4 LUTs	29	1536	1%
Number of bonded IOBs	16	124	12%

Table-4 :Device Utilization Table For 8 bit Conventional Baugh-Wooley Multiplier

Logic Utilization	Used	Available	Utilization
Number of slices	70	768	9%
Number of 4 LUTs	121	1536	7%
Number of bonded IOBs	32	124	25%

VIII. CONCLUSION AND FUTURESCOPE

Conclusion

Analysis of Modified HPM Baugh-Wooley multiplier and conventional methods has been designed and implemented as well as synthesized in Xilinx ISE 13.2 simulator. The simulation result and RTL schematic of the Modified HPM Baugh-Wooley and conventional multiplier is shown in Figure 8.2. The *Baugh-Wooley multiplier* of the delay time is calculated for 4bit is 16.247ns and for 8 bit is 29.27ns.Then the *Modified HPM Baugh-Wooley multiplier* is calculated for 4 bit is 15.36ns and for 8 bit is 27.84ns. From the delay calculation it is found that, the Modified HPM Baugh-Wooley multiplier performs better.

Future scope

Baugh-Wooley multiplier can be compared with performance of other multiplier such as Booth, Dadda, Wallace tree multipliers and also it is possible to reduce the power and delay using HPM. The proposed multiplier can be further extended for 16X16, 32X32 bits. The efficient multipliers can be designed as well as implemented on FPGA and can be used for designingDigital signal processing, VLSI signal processing, Cryptography applications.

REFERENCES

[1] S. Nagarathinamand D . Shanthi, “High Performance Baugh-Wooley Multiplier Using HPM,”ISSN: 2278-3075, Volume-8 Issue-2S2 December, 2018
[2] M. Sjalander and P. Larsson-Edefors, “The Case for HPM-Based Baugh-Wooley Multipliers,” no. 8, p. 16, 2008.
[3] K. D. C. Dandade and P. R. Indurkar, “Design of High Speed 16-Bit Vedic and Booth,” vol. 5, no. Viii, 2017.
[4] R. Kumar and P. Kumar, “An Efficient Baugh-Wooley Multiplication Algorithm for 32-bit Synchronous Multiplication,” vol. 1, no. 2, pp. 28–31, 2014.
[5] J. Antony and J. Pathak, “Design and implementation of high speed baughwooley and modified booth multiplier using cadence RTL,” Int. J. Res. Eng. Technol., vol. 3, no. 8, pp. 56–63, 2014.
[6] AswathySudhakar, D. Gokila VLSI Design Group Department of ECE, “High-Speed Power-Efficient Modified Baugh-Wooley Multipliers”, 978-1-4244-7057-0/10@2010 IEEE.
[7] Andrew D.Booth, “ASigned Binary Multiplication Technique,”QuarterlyJournal of Mechanics and Applied Mathematics,vol 4,pp-236.