Leakage Power Reduction in High Speed Domino Logic Circuits in Deep Submicron Technologies for VLSI Applications

A.Yasodai[1], A.V.Ramprasad[2]
[1]*Department of ECE, Sethu Institute of Technology, Kariapatti-626115, India*
[2]*Department of ECE, K.L.N College of Engineering,Pottapalayam-630612, India*

Abstract - Leakage power and propagation delay are the two major challenges in VLSI design CMOS circuits in small scale technology. This paper proposes a novel technique for designing CMOS domino logic circuits with lector approach and modified inverter for the reduction in leakage power and improved noise performance. NAND and NOR gates are designed with existing and proposed techniques and performances are compared. Designs are tested in 250nm node using TSPICE in CMOS technology at a clock frequency of 5GHz. Simulated results are compared in terms of power consumption and propagation delay. Proposed domino technique has a maximum power reduction from 25% to 80% for different logic circuits and maximum delay reduction from 7% to 20% as compared to the conventional domino logic circuits. Results are proved with TSPICE simulation.

Keywords: domino logic, leakage power , propagation delay, VLSI, CMOS, lector approach

I. INTRODUCTION

Dynamic logic gates are preferred choice in VLSI design due to high speed and less area characteristics as compared to CMOS logic gates with wide fan-in and fan-out[1]. Domino logic circuits are preferred due to their improved noise margin with reduced scaling technology. But it increases the static power consumption. To compensate for that, supply voltage is scaled down. Also threshold voltages are scaled down to achieve performance trade offs. But , scaling of threshold voltage has resulted in exponential increase of static power dissipation by increase of sub threshold leakage current . Reduction in threshold voltage also increases the speed of the domino logic circuits. But noise immunity of the circuit is also decreased[2,3]. Static power dissipation is now growing considerably proportional to the switching dynamic power dissipation in deep submicron technologies and battery operated devices. The longer the battery lasts, the better the leakage power savings[5]-[6].Static power dissipation is mainly due to the leakage current components flowing in the CMOS transistor or CMOS circuits when there is no operation performed on it i.e.during idle or standby mode. It is expected that the leakage power can increase 32 times per device [6] by 2020.The main sources of leakage current in a CMOS transistor are i)Reverse –biased junction leakage current ii) Gate induced drain leakage iii) Gate direct-tunneling leakage iv)Subthreshold leakage current(weak inversion).Therefore , leakage currents, noise sources and low threshold voltage degrade the performance of the circuit at high frequencies[4].
Power consumption in VLSI circuits are of three types[7,8,9]

$$P_g = P_{short} + P_{dynamic} + P_{leakage}$$

Where ,
P_{short}- short circuit power dissipation when both pmos and nmos are grounded at a time in series.
$P_{dynamic} = \alpha V_{dd}^2 f$

- α -switching activity (charging and discharging of load capacitance)
V_{dd}– supply voltage
f- clock frequency
$P_{leakage}$- power consumed due to gate and sub threshold leakage current
Device dimensions and supply voltage are scaled down to reduce power consumption in CMOS logic circuits. Scaling of device leads to increase of leakage current due to unwanted short channel effects. Effective channel length and threshold voltage has been reduced due to this short channel effect[10,11,12].

Already various techniques have been proposed to reduce leakage current in domino logic circuits[7,8,9]. These techniques are modified form of footer less logic and footed logic in domino logic circuits. This paper proposes a modified domino logic with modified inverter al to improve power consumption , propagation delay , noise immunity and noise margin.This paper discusses the existing technique of High Speed Clocked Delay domino

logic style in section 2. Proposed High Speed Clocked Delay domino logic is discussed in section 3. Both existing and proposed techniques are designed and tested in 250nm CMOS technology. Results are discussed in section 4.

II. HIGH SPEED CLOCKED DELAY FOOTED DOMINO LOGIC

In High-Speed-Clocked Delay(HSCD)[7,13] circuit shown in Fig 1,at the beginning of precharge node, transistor N1 is ON. Therefore transistor N1 connects node N to ground.N2 transistor was switched off by node GN which is at low voltage. Transistor N1 turns off after a delayequal to delay of two inverters. Consequently voltage at node N increases and also sizing of the evaluation logic transistor is selected in such a way that node GN remains low compared to V_{th} of N2. Because of this consecutive action , N2 transistor remains off in precharge mode. In evaluation mode, voltage at node N is increased due to N1 switch off. It increases the biasing of N1 transistor in evaluation logic which leads to reduce leakage power consumption. The speed of the logic increaseson increasing the size of N1, N2 or evaluation transistors. The voltage at node N decreases with increase in size of N1 and increases[14] with increase in size of evaluation transistors.

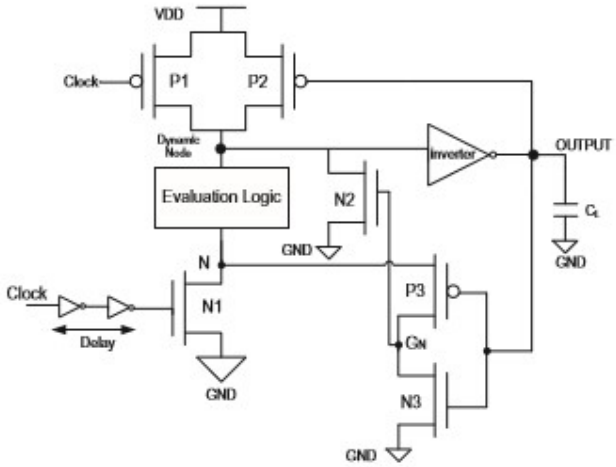

Fig 1- High-speed Clocked delay Domino Logic (HSCD).

In HSCD technique, an AND gate G and NMOS transistor are added to increase the speed of evaluation logic. This circuit is modified form of HSCD technique [7]. Therefore it is termed as modified HSCD technique shown in Fig 2. In M-HSCD technique , dynamic node discharges when one or more inputs high during evaluation mode. At this time input A to gate goes high, but for input B to gate goes high after two inverter delays. Therefore it turns on the transistor MD. In this way evaluation speed increases, but one problem is with AND gate output remains with zero. This is solved in the proposed technique.

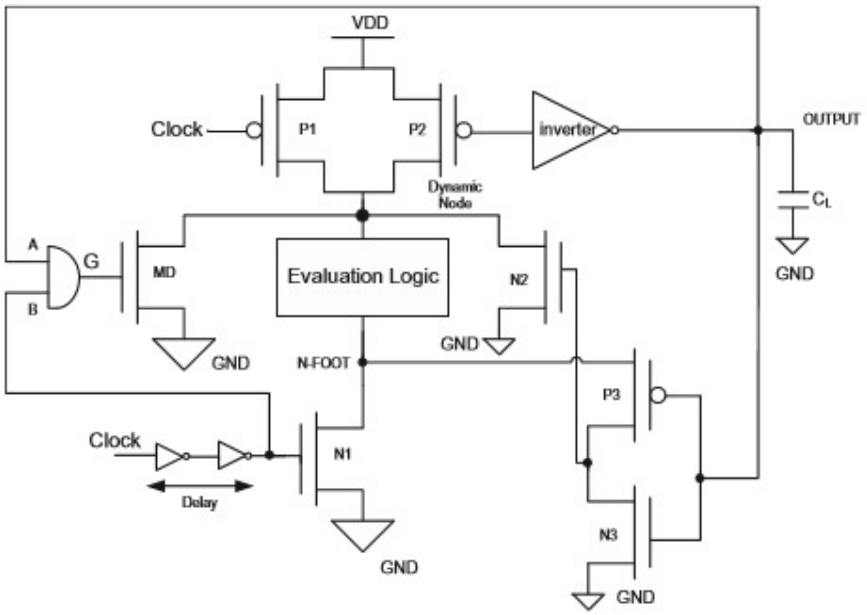

Fig-2 Modified High-speed Clocked delay Domino Logic (M-HSCD).

III. PROPOSED HIGH SPEED DOMINO LOGIC

Section 2 describes various technique for designing high speed domino logic circuits. This section proposes new technique for designing domino logic circuit. This technique is termed as Lector based foot driven stacked transistordomino logic which is shown in Fig 3.

In Lector technique, two leakage control transistors (PMOS and NMOS) are introduced [15] between the pull-up network and pull-down network within the logic circuit shown in fig 4. These transistors are connected as such that one of the transistor is always near the cut-off voltage for any input combination. This increases the path resistance from supply to ground, leading to significant reduction of leakage currents. The Lector technique works effectively in both active modes as well as in the standby mode.

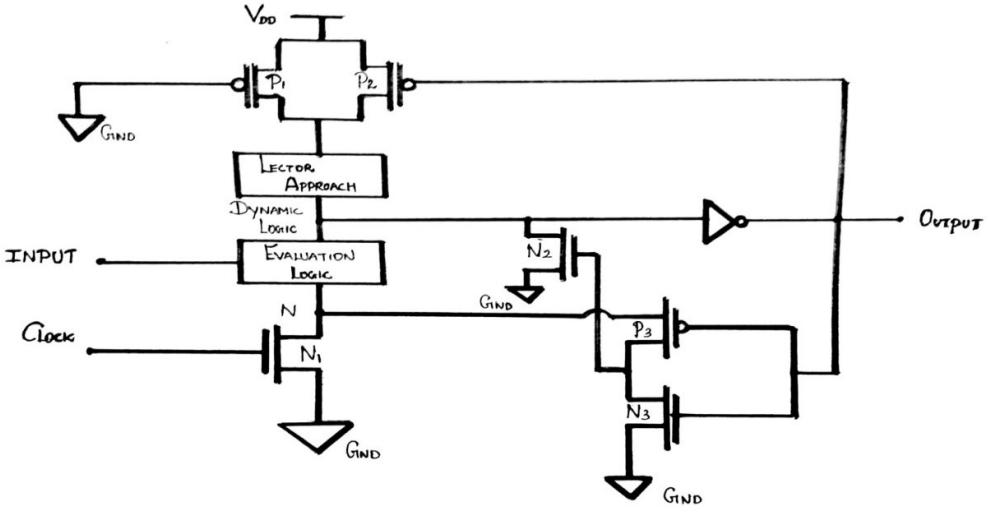

Fig 3 Proposed Lector based foot driven stacked transistor domino logic

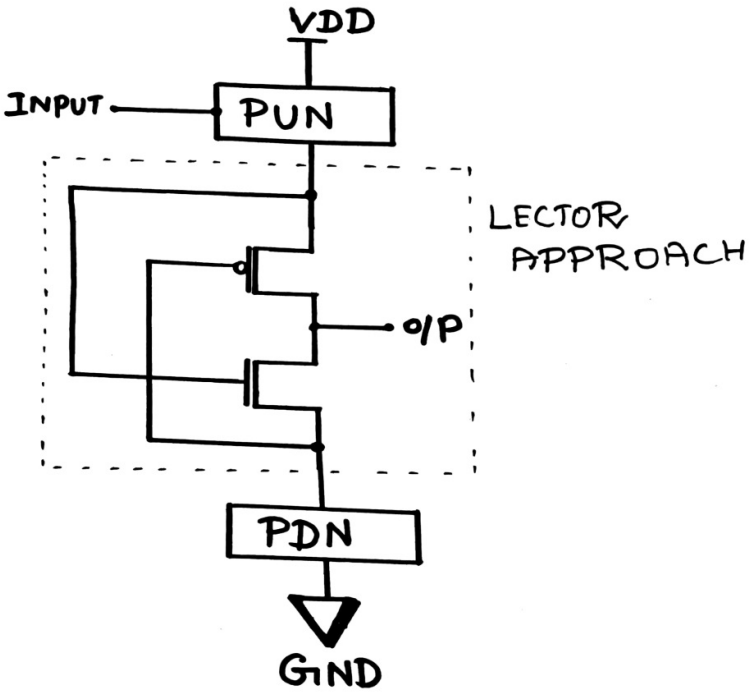

Fig 4 Lector Approach

Here the gate node of N1 have not given with the two delay elements of the inverter and we have set the lector approach in between the PUN transistor and the evaluation logic and the inverter input is connected in between the output of the lector approach and input of the evaluation logic. The N2 transistor input is driven to input of the inverter. The circuit has two sections, input section has a PMOS pre-charge transistor P1, evaluation network consisting of NMOS transistors in parallel anda footer transistor N1 whereas output section comprises of keeper transistor P2, static inverter and stacked NMOS transistors N2 and N3. The inputs to the circuit are applied through gate of the NMOS transistors in evaluation network. Transistor N2 is driven by the voltage at the foot N of evaluation net-work whereas transistor N3 is driven by the output voltage.

Transistors N2 and N3 are used in a stack configuration. Whenever there is a voltage drop across N1 due to noise pulses, transistor N3 provides stacking effect by lector approach of N2 smaller. This will reduce the leakage power of N2 and makes N1 conduct less.

3.1 AND Gate using proposed Logic

Two input AND Gate using proposed technique is shown in Fig 5. In AND gate , evaluation logic transistors are connected in series. During pre-charge phase , the output of the circuit remains high. During evaluation phase, dynamic node output changes according to input changes. The output waveform of two input AND gate for different combination of input is shown in Fig 6

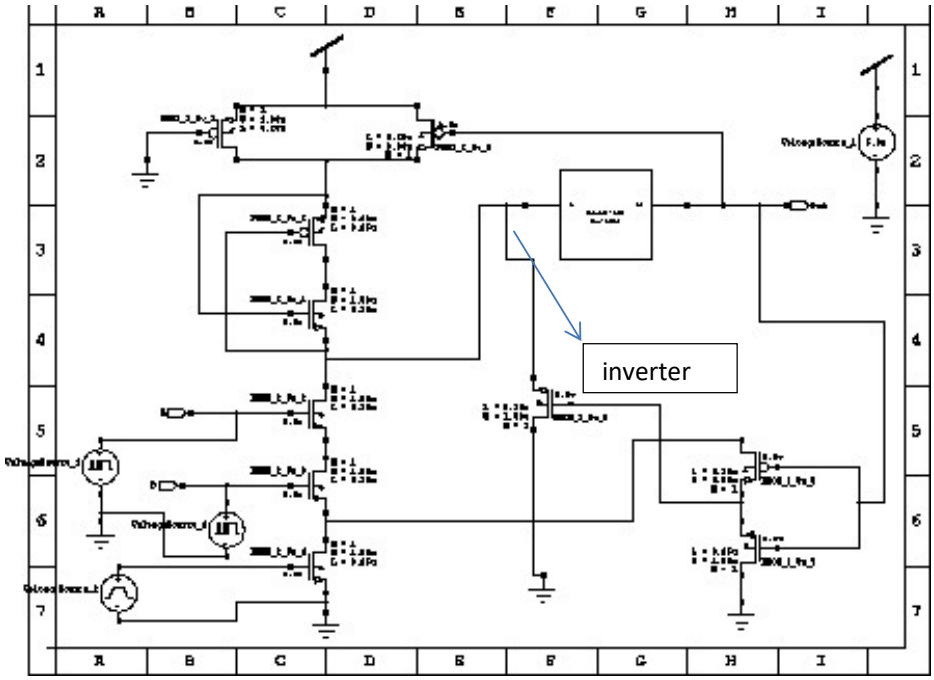

Fig 5 AND Gate Using Proposed Logic

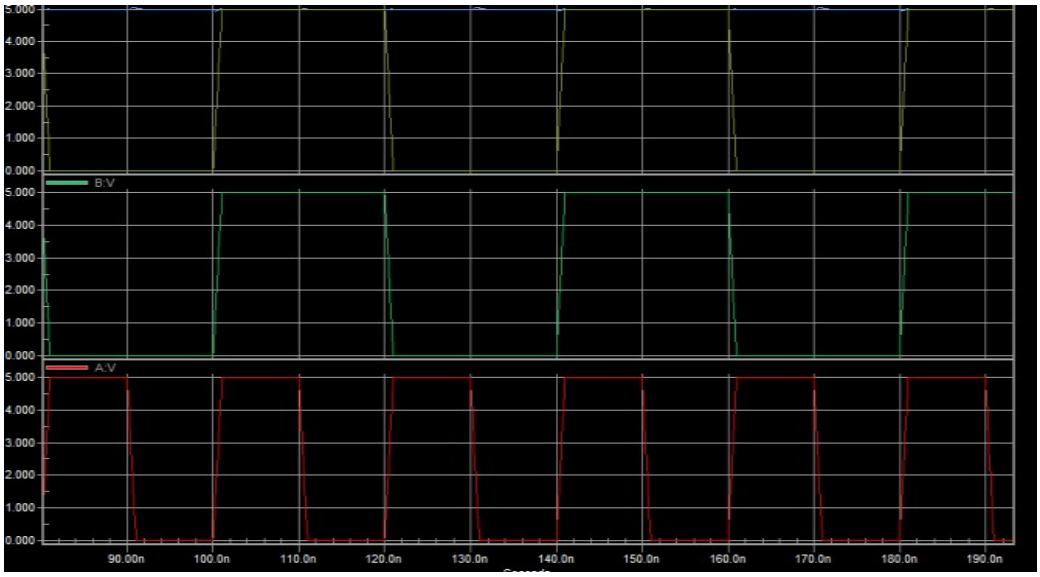

Fig 6- Output Waveform for Two input AND Gate with proposed logic

3.2 OR Gate Using Proposed Logic

Two input OR Gate using proposed technique is shown in Fig 7. In AND gate , evaluation logic transistors are connected in parallel. During pre-charge phase , the output of the circuit remains high. During evaluation phase, dynamic node output changes according to input changes. The output waveform of two input OR gate for different combination of input is shown in Fig 8

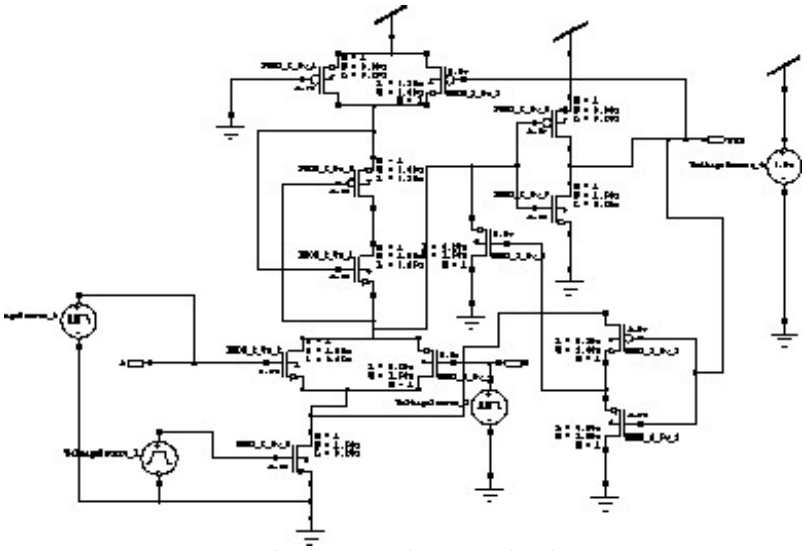

Fig 7 OR Gate Using Proposed Logic

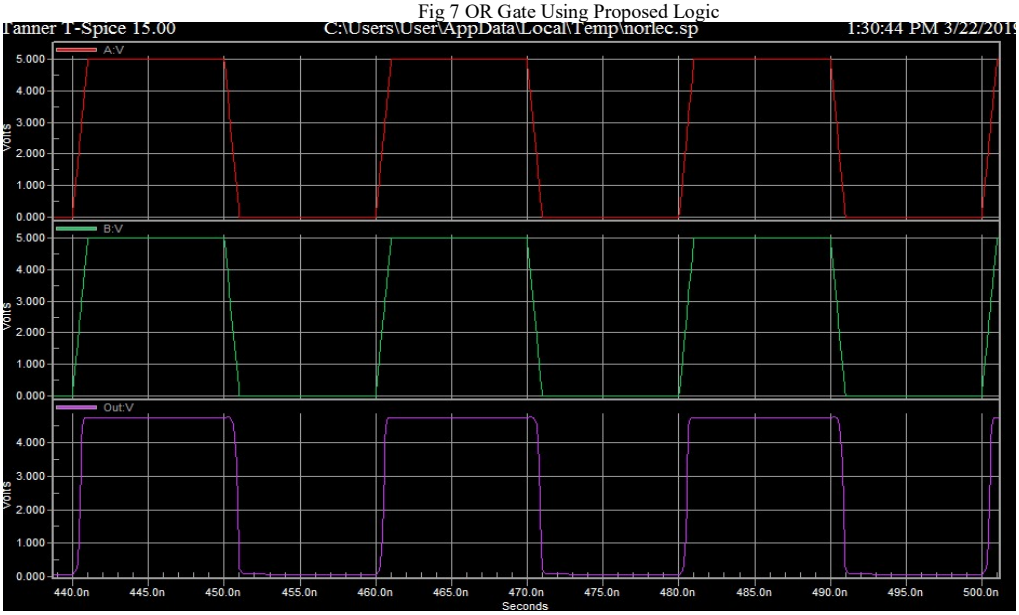

Fig 8 Output Waveform of OR Gate for different Combinations of Input

V. RESULTS AND DISCUSSION

Proposed Lector based foot driven stacked transistor domino logictechnique and without Lector based foot driven stacked transistor domino logic styles are simulated in 250nm CMOS technology. Two input OR , AND gates are implemented in TSPICE. Various metrics have been measured to measure robustness and noise immunity of the gates. The metrics used in this paper are

i)Average Power:

Average power(P_{av}) is calculated by transient analysis of the circuit. In this , transient analysis is done for a time span of 100ns. The frequency of the clock is set as 5GHz for transient analysis.

ii) Propagation delay:

Propagation delay of the circuit(t_{pd}) of the circuit is the time taken by the signal from input to output. Delay determines the speed of the circuit. When the circuit enters the evaluation phase , delay is measured.

$t_p = (t_{pHH}+t_{pLL})/2$

t_{pHH}-delaybetween 50% rising input and rising output

t_{pLL}-delay between 50% falling input and falling output

Table 1 shows the comparison of average power consumption and propagation delay for various gates:

Table 1 Comparison of average power Consumption and Propagation delay

Gate	Power (Pav) with lector	Power (Pav) without lector	Propagation delay (t_p) with lector	Propagation delay(t_p) without lector	% improvement in power	% improvement in delay
AND Gate	2.155mW	7.53mW	40.148nS	50nS	83.01	20.1
OR Gate	3.59mW	4.85mW	183.69ns	200.2nS	24.6	7

iii)Noise Margin:
Noise margin is the amount of **noise** that a CMOS circuit could withstand without compromising the operation of circuit. **Noise margin** does makes sure that any signal which is logic '1' with finite **noise** added to it, is still recognised as logic '1' and not logic '0'.Noise Margin Results are shown in Table 2.

Table 2 Comparison of Noise Margin with proposed technique

VI-INPUT/OUTPUT	**AND Gate (With Lector)**	**AND Gate (Without Lector)**	**OR Gate (With Lector)**	**OR Gate (Without Lector)**
VI-HIGH	5V	5V	5V	5V
VO-HIGH	4.6V	5V	4.7V	4.6V
VI-LOW	0V	0V	0V	0V
VO-LOW	0.2V	1.2V	0.2V	0.1V

Table 1& 2 shows the simulation results for 2 input AND gate and OR gate using with and without Lector approach for foot driven stacked transistor domino logic. Table 1 & 2 proves that proposed technique has better performance in terms of power(P_{av}) , propagation delay
(t_p) and Noise Margin.

VI. CONCLUSION

This paper proposes a new lector based approach for designing domino logic circuits with reduced leakage power consumption, propagation delay with improved noise performance characteristics in stacked transistor domino logic. The proposed design is compared with existing High speed domino technique in 250nm CMOS technology on the basis of power and delay at a clock frequency of 5GHz.. With proposed technique ,AND Gate hasupto 83.01% power improvement and 20 % delay improvement . OR Gate hasupto 20% power improvement and 7% delay improvement. The noise marginwasreducedattherangeof4.4V-4.6Vanditwasobtainedat4.6V.Meanwhile, the noise margin in the NOR GATE was obtained above 4.7V -5V but here the the noise margin was obtained at 4.7V. It will optimize the power consumption and the time period to complete the process of a task so it will reduce the heat dissipated in an IC and it will improve the speed and synchronisation of thecycle.

REFERENCES

[1] M. Jhumb, Gitanjali Efficient Adders for assitive devices space, Eng. Sci. Technol. Int. J. 20 (1) (2017) 95–104.
[2] M. Anis, S. Areibi, M. Elmasry, Design and optimization of multi-threshold CMOS (MTCMOS) circuits, IEEE Trans. Comput. Aided Design Integr. Circuits Syst. 22 (10) (2003) 1324–1342.
[3] K. Roy, S. Mukhopadhyay, H. Mahmoodi, Leakage current mechanisms and leakage reduction techniques in deep-submicron CMOS circuits, Proc. IEEE 91(2) (2003) 305–327.
[4] H. Choi, B.C. Paul, K. Roy, Dynamic Noise Analysis with Capacitive and Inductive Coupling, in: Proceedings of 7th Asia and South Pacific Design Automation Conference(ASPDAC), 2002, Jan 11.
[5] De and S.Borkar, "Technology and design challenges for low power and high performance," in Proc. Int. Symp. Low Power Electroics and Design, 1999, pp.163-168.
[6] K.Roy and S.C.Prasad, "Low-power CMOS VLSI ciruit design". New York: Wiley, 2000, ch. .5, pp.214-219.
[7] F. Moradi, T.V. Cao, E.I. Vatajelu, A. Peiravi, H. Mahmoodi, D.T. Wisland, Domino logic design for high performance and leakage-tolerant applications, Integr. VLSI J. 46 (3) (2013) 247–254.

[8] F. Moradi, H. Mahmoodi, A. Peiravi, A high speed and leakage-tolerant domino logic for high fan-in gates, Proceedings of the 15th ACM Great Lakes Symposium on VLSI (GLSVLSI), 2005, Chicago, IUSA, Apr. 17–19
[9] A. Dadoria, K. Khare, T.K. Gupta, R.P. Singh, A novel high-performance leakage tolerant Wide Fan-In Domino Logic Circuit in deep Sub-micron technology, Circuit Syst. 6 (4) (2015) 103–111.
[10] S.M. Sharroush, Y.S. Abdalla, A.A. Dessouki, Impact of technology scaling on the performance of domino CMOS logic, in: International Conference on ElectronicDesign 2008, Dec. 1 –3.
[11] M. Jhumb, Garima, H. Lohani, Design implementation and performance comaprison of multiplier topologies in Power-delay space, Eng. Sci. Technol.Int. J. 19 (1) (2016) 355–363.
[12] M.H. Moaiyeri, M. Nasiri, N. Khastoo, An Efficient ternary serial adder based on carbon nanotube FETs, Eng. Sci. Technol. Int. J. 19 (1) (2016) 271–278.
[13] F. Moradi, H. Mahmoodi, A. Peiravi, A high speed and leakage-tolerant dominologic for high fan-in gates, Proceedings of the 15th ACM Great LakesSymposium on VLSI (GLSVLSI), 2005, Chicago, IUSA, Apr. 17–19.
[14] SandeepGargĥ, Tarun Kumar Gupta, “Low power domino logic circuits in deep-submicron technology using CMOS” , Engineering Science and Technology, an International Journal 21 (2018) 625–638
[15] NarenderHanchateand and NagarajanRanganathan, “LECTOR: A Technique for Leakage Reduction in CMOS Circuits,” IEEE Transactions on VLSI Systems, vol. 12, no. 2, Feb 2004, pp.196-205.